Measuring Moore's Law:

Evidence from Price, Cost, and Quality Indexes

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"Moore's Law" in the semiconductor manufacturing industry is used to describe the predictable historical evolution of a single manufacturing technology platform ("silicon CMOS") that has been continuously reducing the costs of fabricating electronic circuits since the mid-1960s. Some features of its future evolution were first correctly predicted by Gordon E. Moore (then at Fairchild Semiconductor) in 1965, and Moore's Law became an industry synonym for continuous, periodic reduction in both size and cost for electronic circuit elements.

Technological innovation for this manufacturing platform was coordinated and synchronized across a variety of different engineering fields, including materials, optical systems, ultraclean precision manufacturing, factory automation, electronic circuit design and simulation, and improved computer software for computational modelling in all of these fields. It was a self-reinforcing dynamical process, since the largest market for the semiconductor manufacturing industry's products has always been the computer industry.[2] Cheaper computing hardware meant cheaper modeling and engineering to further reduce the costs of the semiconductors manufactured for use in future computers. New public-private institutions and organizations were developed to coordinate the simultaneous arrival of the very heterogeneous technological building blocks required for this increasingly complex semiconductor manufacturing technology platform.

The result was an industrial dynamic that, since the mid-1960s, had effectively worked as a "virtual shrinking machine" for electronic circuits. On a regular basis, new "technology nodes" delivered 30 percent reductions in the size of the smallest dimension ("critical feature size," F) that could be reliably manufactured on a silicon wafer. This implied a 50 percent reduction in the area occupied by the smallest manufacturable electronic circuit feature (F^2), and a doubling in density—the number of circuit elements (e.g., transistors) per area of silicon in a chip. Section 1 develops some stylized economic facts, reviewing why this progression in manufacturing technology delivered a 20 to 30 percent annual decline in the cost of manufacturing a transistor, on average, as long as it continued.

Section 2 reviews other economically significant benefits (in addition to increased density and lower cost per circuit element) that would be associated with smaller feature sizes. Some of those characteristics would be expected to have significant economic value, and historical trends for these characteristics are reviewed. Chip speed, in particular, would have major impacts on computer

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[2] Defining the computer industry expansively, to include the computer systems embedded in the smart electronic systems and mobile devices whose sales have grown most rapidly in recent decades.

performance. Econometric analysis of software benchmark data shows rates of performance improvement in CPUs declining dramatically in the new millennium, a retreat from very high rates of increase measured in the late 1990s. Lower manufacturing costs alone pose no special challenges for price and innovation measurement, but these other benefits do, and motivate quality adjustment methods when semiconductor product prices are measured.

Section 3 analyzes empirical evidence of recent changes to the historical Moore's Law trajectory, and finds corroborating evidence for a slowdown in Moore's Law in prices for the highest volume products: memory chips, custom chip designs outsourced to dedicated contract manufacturers (foundries), and Intel microprocessors. Section 4 reviews evidence to the contrary, which relates primarily to Intel microprocessors, and discusses economic reasons why Intel microprocessor prices might behave differently from prices for other types of semiconductor chips.

Section 5 dives into microprocessors in greater depth, and tests the computer architecture textbook view of how a small set of specific chip characteristics affect performance of microprocessors in executing programs, by outlining a structural model of microprocessor computing performance, then estimating that model empirically. This simple econometric model, using only a small set of explanatory chip characteristics, explains 99% of variance across processor models in performance on commonly used CPU performance benchmarks. These characteristics, which determine benchmark scores, should clearly be included in any hedonic price equation. Most of these chip characteristics would also be expected to affect chip production cost, and would therefore have an additional rationale for inclusion in a hedonic price equation supplanting their role in determining computer performance benchmark scores.

1. Stylized Facts About Semiconductor Manufacturing Innovation

In 1965, five years after the integrated circuit's invention, Gordon E. Moore (who would shortly move on to co-found Intel) predicted that the number of transistors (circuit elements) on a single chip would double every year.[3] Later modifications of that early prediction—"Moore's Law"—became shorthand for semiconductor manufacturing innovation.

Moore's prediction requires other assumptions in order to create economically meaningful connections to the information age's key economic variable: the cost (or price) of electronic functionality on a chip (embodied in the 20th century's supreme electronic invention, the transistor).[4] Chip fabrication requires coordinating multiple technologies, combined in very complex manufacturing processes.

The pacing technology has been the photolithographic processes used to pattern chips. From the 1970s through the mid-1990s, a new "technology node"— a new generation of photolithographic and related equipment, and materials required for successful use—was introduced roughly every three years or so. Starting in the mid-1970s, this three year cycle coincided with the time interval between introductions of next-generation DRAM computer memory chips, storing four times the bits in the

[3] G. Moore (1965).

[4] Jorgenson (2001), Flamm (2003), (2004); Aizcorbe, Flamm, and Khurshid, (2007).

previous generation chip.[5] This observed 18-month "doubling period" became a new, *de facto*, "revised" Moore's law.[6]

The close early fit of DRAM product development cycles with leading edge chip manufacturing technology introductions was no coincidence. DRAMs at that time were the highest volume, standardized, commodity chip product manufactured, and a rapidly expanding computer market drove leading edge chip manufacturing technology development. Moore's prediction morphed into an informal, and later, formal technology coordination mechanism (the International Technology Roadmap for Semiconductors, or ITRS) for the entire global semiconductor industry—equipment and material producers, chip makers, and their customers.

Relationships between Moore's Law and fabrication cost[7] trends for integrated circuits can be described by the following identity, giving cost per circuit element (e.g., transistor):

$$(1)\ \$/\text{element} = \frac{\$\ \text{processing cost}}{\text{area "yielded" good silicon}} \times \frac{\text{silicon wafer area}}{\text{chip}} \Big/ \text{elements/chip}$$

Moore's original "Law" described only the denominator—a prediction that elements per chip would quadruple every two years. Back in 1965, Moore hadn't originally anticipated rapid future advances in technology nodes. Acknowledging that an IC containing 65,000 elements was implied by 1975, Moore wrote: "I believe that such a large circuit can be built on a single wafer. With the dimensional tolerances already being employed…65,000 components need occupy only about one-fourth a square inch."[8]

Rewriting this more concisely without relying on Moore's prediction about numbers of elements per chip (therefore eliminating the need for assumptions about chip size):

$$(2)\ \$/\text{element} = \frac{\$\ \text{processing cost}}{\text{area yielded silicon}} \times \frac{\text{silicon area}}{\text{element}}$$

which depends directly on the defining characteristic of a new technology node, smallest patternable feature size, as reflected in chip area per transistor. This "Moore's Law" variant came into use in the semiconductor industry as a way of analyzing the economic impact of new technology nodes. New technology nodes increased density of transistors fabricated in a given area of silicon in a readily predictable way. Time between new nodes—and a new node's impact on wafer processing costs—jointly determined decline rates in transistor fabrication cost.

Through 1995, new technology nodes were introduced at roughly three year intervals. Each new node reduced the smallest planar dimension ("critical feature size," F), in circuit elements by 30%, implying 50% smaller silicon areas (F^2) per circuit element.

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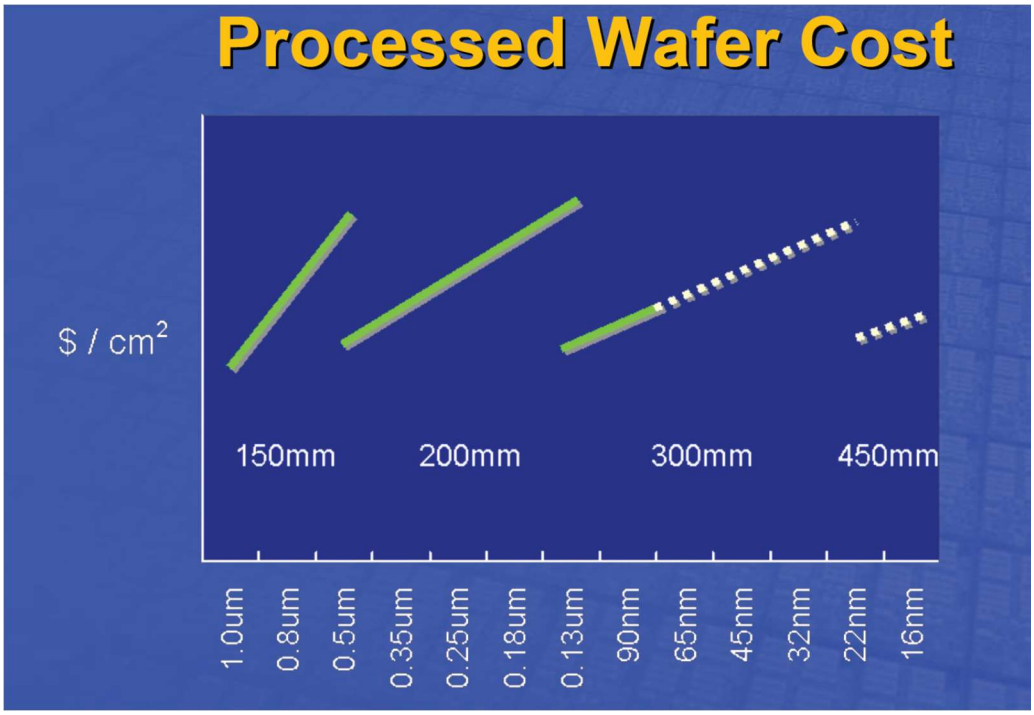
[5] The DRAM memory was invented in 1968 by Robert Dennard at IBM, and first commercialized by Moore's newly founded company, Intel, in 1970.

[6] A decade later, Moore himself revised his prediction to a doubling every two years. G. Moore (1975), pp. 11–13.

[7] Analysis of fabrication costs, which account for most chip cost, ignores assembly, packaging, and test.

[8] Moore (1965). The largest wafer sizes in use then were comparable in diameter to a modern snack mini-pizza appetizer.



Source: Holt (2005).

Figure 1. Wafer size conversions offset Intel's increased wafer-processing cost

Completing the economic story, cost per silicon wafer area processed, averaged over long periods, increased only slowly.[9] At new technology nodes, processing cost per silicon wafer area indeed increased. But, episodically, larger wafer sizes were introduced, sharply reducing processing costs per area. The net effect was nearly constant long run costs, with only slight increases. Figure 1, presented in 2005 by Intel's chief manufacturing technologist, shows new wafer sizes "resetting" wafer-processing costs. Significantly, larger diameter wafer sizes (450mm) were expected at the 22 nanometer (nm) node. However, 450mm wafers were not introduced as Intel adopted 22nm technology in 2012, had not been introduced by 2017, and even future introduction now seems highly uncertain. The most recent wafer size "reset," adoption of 300mm diameter wafers, occurred at the 130nm technology node, around 2002.

Using these stylized trends—wafer-processing cost per area of silicon roughly constant, and silicon area per circuit element halved with new technology nodes introduced every three years—equation (2) above predicts that every three years, the cost of producing a transistor would fall by 50%, a 21% compound annual decline rate.

In reality, leading edge computer chips—like DRAM memory (the primary product originally produced at Intel after Moore and others founded that company, which immediately became the largest volume product in the semiconductor industry and the primary product driving Intel's initial growth)—

[9] Over 1983-1998, wafer-processing cost/cm^2 silicon increased 5.5 percent annually. Cunningham et. al. (2000), p. 5. This estimate relates to total silicon area processed (including defective chips). Since defect-free chips' share of total processed area increased historically (chip fabrication yields increased), wafer-processing cost per good silicon area rose even more slowly, approximating constancy.

dropped in price substantially faster than 20% pre-1985. The steeper decline rate in part reflected further increases in density due to circuit design improvements (e.g., reduction in memory cell footprint)[10], 3-D interconnect layers enabling tighter packing of circuit elements,[11] and gradual introduction of 3-D into physical designs of transistors and other circuit elements.[12] In addition, operating characteristics of a given circuit design—in particular, switching speed and power requirements—improved with new manufacturing technology, and made additional contributions to quality-adjusted price. Finally, smaller and cheaper transistors made it economic to add ever greater electronic functionality to chips, and more and more of a complete electronic system was progressively integrated onto a single chip, which greatly improved system reliability.[13]

In the mid-1990s, the semiconductor manufacturing industry arrived at a significant technological inflection point.[14] New technology nodes began arriving at two-year intervals, replacing three-year cycles. (Intel's perception of this trend, as of 2005, is documented in Figure 2.) The origins of this change lie in the early 1990s, when the U.S. SEMATECH R&D consortium sponsored a roadmap coordination mechanism in pursuit of an acceleration in the introduction of new manufacturing technology, intended to benefit the competitiveness of US chip producers. By the mid-1990s, with the increasing reliance of semiconductor manufacturing on a global industrial supply chain, the American national roadmap evolved into the international ITRS.[15] Explicitly coordinating the simultaneous development of the many complex technologies required to enable a new manufacturing technology node every two years apparently succeeded in raising the tempo of semiconductor manufacturing innovation for over a decade.[16]

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[10] Flamm (2010), Figure 2, documents a 62 percent decline in minimum memory bit cell footprint between 1995 and 2004.

[11] Anticipated by Moore back in 1965: "no space wasted for interconnection…using multilayer metallization patterns separated by dielectric films." Moore (1965).

[12] Recent examples of 3-D transistor structures include RCAT (recessed cell array transistor) and FinFET (fin field effect transistor) structures. 3-D capacitor designs have been used in DRAM since the late 1990s.

[13] Since electrical interconnections between components have historically been the most frequent point of failure in electronic systems.

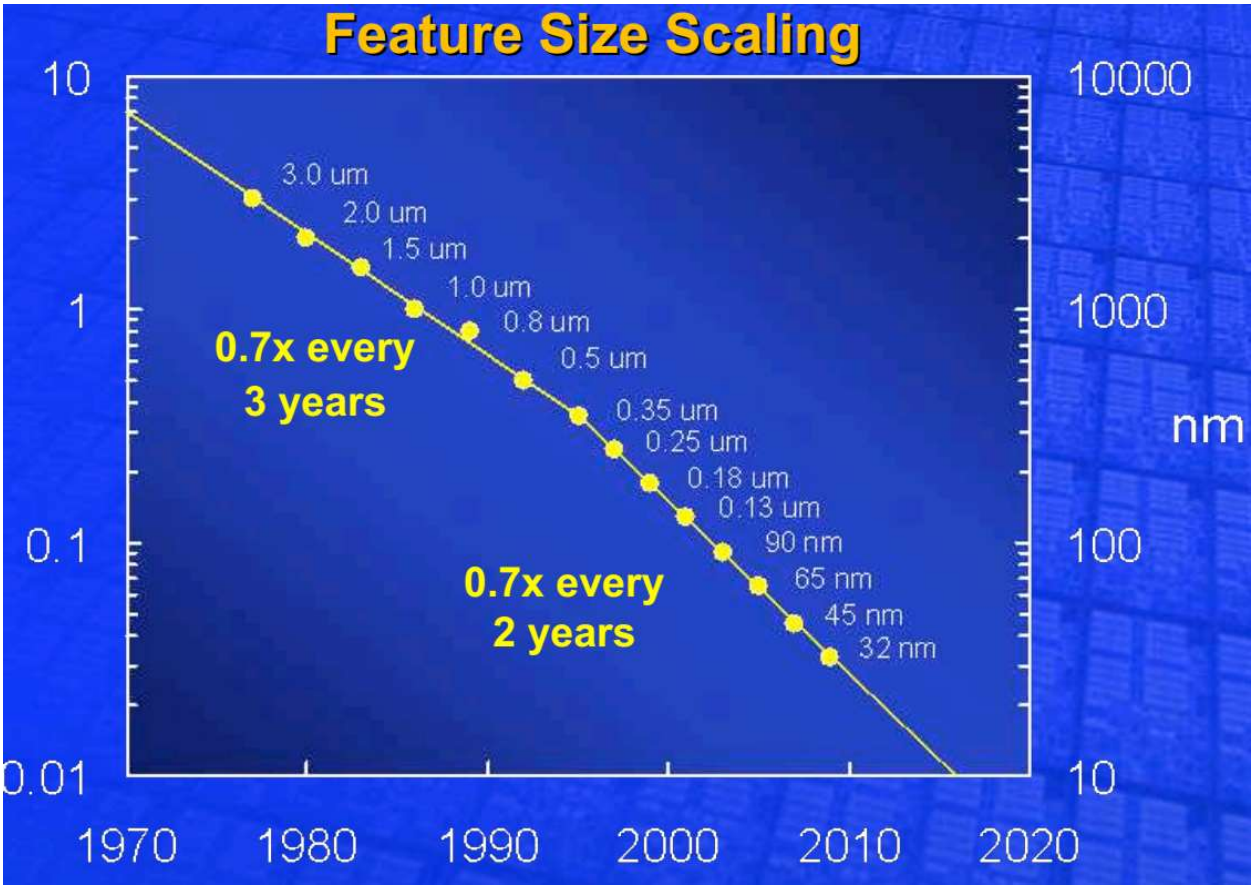
[14] Industry roadmaps originally dated this transition to two-year node rollouts to 1995; post-2004 roadmaps revised that date to 1998. Aizcorbe, Oliner, and Sichel, (2008) have persuasively argued that the turning point was closer to mid-1990s than late in the decade.

The mid-1990s were also a technological inflection point for Intel's manufacturing capabilities. Intel had exited the DRAM business in 1985, which previously had been driving its leading edge manufacturing technology development, and refocused its R&D on logic circuit design. Burgelman (1994), pp. 32-46. As a consequence, by the late 1980s, Intel manufacturing capability was trailing well behind the leading edge of the manufacturing technology it had once pioneered.

In order to catch up, Intel began adopting new nodes every two years, even as the rest of the industry continued at the historical three-year pace. Comparing launch dates for Intel processors at new technology nodes with initial use of those nodes by DRAM makers: Intel was 2 years behind in 1989 (at 1000nm); 3 years behind in 1991 (800nm); 1 year behind in 1995 (350nm). Intel caught up with the DRAM makers in 1997, at 250nm, and remained on a roughly 2-year cycle through 2014. Author's calculations based on Intel (2008), IC Knowledge (2004), http://ark.intel.com.

[15] Flamm (2009); Spencer and Seidel (2004).

[16] The last (incomplete) official roadmap prepared by ITRS was released in 2012. Intel and others reportedly withdrew from ITRS around this time.



Source: Holt (2005).

Figure 2. Feature size scaling as observed by Intel in 2005

Using (2), but adopting shorter two-year cycles for new technology nodes, implies rates of annual decline in transistor cost accelerating to almost 30%. In short, if the historic pattern of 2-3 year technology node introductions, combined with a long run trend of wafer processing costs increasing very slowly were to have continued indefinitely, a minimum floor of perhaps a 20 to 30 percent annual decline in quality-adjusted costs for manufacturing electronic circuits would be predicted, due solely to these "Moore's Law" fabrication cost reductions. On average, over long periods, the denser, "shrink" version of the same chip design fabricated year earlier would be expected to cost 20 to 30 percent less to manufacture, purely because of the improved manufacturing technology.

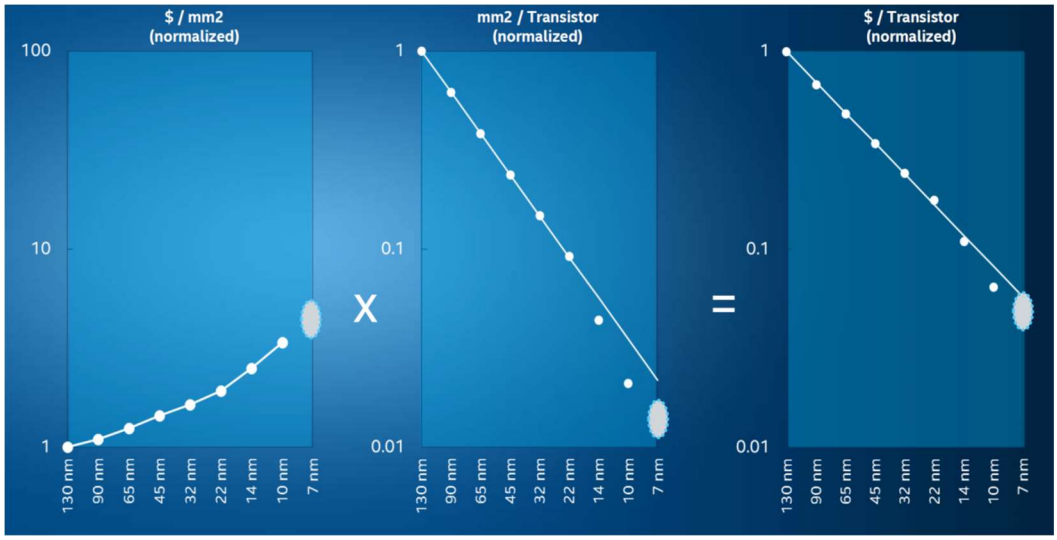
It now appears that this two-year cycle for technology nodes definitively ended in 2014, with deployment of the 14nm node. The most historically prominent adopter of leading edge chip manufacturing technology, Intel, currently projects a delayed introduction of its next 10nm processor products to no earlier than late 2019.[17] This means that time between introductions of new technology nodes now is approaching ***5*** years for Intel, a dramatic change from its two-year cadence through 2014.[18]

[17] See http://wccftech.com/intel-delays-10nm-cannon-lake-cpus-end-2018/ .

[18] Intel chip manufacturing competitor TSMC was said in early 2017 to be manufacturing a "10nm" node in volume for Apple (See R. Merritt, "TSMC, Samsung Diverge at 7nm," *EE Times*, Feb. 8, 2017, (http://www.eetimes.com/document.asp?doc_id=1331324), but it is widely believed in the industry that its

At Intel, the post-1995 two-year technology development cycle had been explicitly incorporated into marketing efforts, and dubbed the Intel "tick-tock" development model in 2007.[19] Every two years, there would be a new technology node introduced ("tick"), with the existing microprocessor computer architecture ported to the new node (effectively "die shrinks" using the new process), followed by an improved architecture fabricated with the same technology the following year ("tock"). The death of the "tick-tock" model was officially acknowledged by Intel in its 2016 annual report.[20]

Intel publicly disclosed a version of equation (2) to its shareholders in 2015, purged of sensitive cost numbers by indexing all variables to equal one at the 130nm technology node, the technology node at which the transition to a larger wafer size occurred.[21] The 2015 Intel decomposition of manufacturing cost per transistor, using equation (2), is shown as Figure 3, and in Table 1. Generally, Intel's average silicon area per transistor did not decline by the predicted 50% between technology nodes, primarily because of the increasing complexity of interconnections in processor designs.[22] If accurate, these numbers indicate average chip area per transistor shrank by 38% at each new node from 130nm through 22nm.[23] Nor did Intel's wafer-processing costs stay constant over the post-130nm period as a whole, since the adoption of 450mm wafers, and subsequent cost reset, never happened at 22nm, as had been predicted back in 2005. However, as long as average area per transistor declined at faster rates than processing costs per area increased, transistor cost would continue to decline. Intel's cost per transistor estimates are revisited below.



Source: Holt (2015).

current technology is physically equivalent to a half node advancement over the previous generation Intel technology node. See https://www.semiwiki.com/forum/f293/intel-tsmc-samsung-10nm-update-8565.html ; http://wccftech.com/intel-losing-process-lead-analysis-7nm-2022/ ; Rogoway (2018); Cuttress and Shilov (2018).

[19] See http://www.intel.com/pressroom/archive/releases/2007/20070918corp_a.htm .

[20] Intel (2016), p. 14.

[21] Intel actually produced microprocessors in volume on both 200mm (8") and 300mm (12") wafers using its 130nm manufacturing process technology. See Natrajan, at. al., (2002), pp. 16-17.

[22] See Flamm (2017), p. 34, for a more detailed explanation.

[23] Absolute constancy in reported decline rates for average area per transistor over five generations of new Intel manufacturing technology is puzzling, suggesting long-run trend-based estimates rather than actual averages computed from empirical manufacturing data.

Figure 3. Intel 2015 version of equation (2)

							Compound Annual Percentage Change:		
Year Intel 1st Shipped New Product at Tech Node	**Tech Node (nm)**	**Wafer Processing Cost ($ / mm²)**	**X**	**Transistor size (mm² / transistor)**	**=**	**$ Cost / Transistor**	**Wafer Processing Cost ($ / mm²)**	**Transistor size (mm² / transistor)**	**$ Cost / Transistor**
2002	130	1		1		1			
2004	90	1.09		0.62		0.68	5%	-21%	-18%
2006	65	1.24		0.38		0.47	7%	-21%	-16%
2008	45	1.43		0.24		0.34	7%	-21%	-15%
2010	32	1.64		0.15		0.24	7%	-21%	-16%
2012	22	1.93		0.09		0.18	8%	-21%	-14%
2014	14	2.49		0.04		0.11	14%	-31%	-22%
Source: Bill Holt, "Advancing Moore's Law," presentation to Intel Investor Meeting, 2015, Santa Clara, slide 6, graph digitized using WebPlotDigitizer. Year node introduced from ark.intel.com .									

Table 1. Decomposing Intel Transistor Cost Declines into Wafer Cost and Transistor Size Changes

How would reductions in production cost translate into price declines? One very simple way to think about it would be in terms of a "pass-through rate," defined as dP/dC (incremental change in price per incremental change in production cost). The pass-through rate for an industry-wide decline in marginal cost is equal to one in a perfectly competitive industry with constant returns to scale, but can exceed or fall short of 1 in imperfectly competitive industries. Assuming the perfectly competitive case as a benchmark for long-run pass-through in "relatively competitive" semiconductor product markets, this would then imply an expectation of 20-30% annual declines in price, due solely to Moore's Law.

Historically, most semiconductor chip production ultimately seems to have migrated to more advanced technology nodes.[24] Other kinds of innovations in semiconductor manufacturing, or innovations in the design and functionality going into electronic circuits, might be expected to stimulate even greater rates of quality-adjusted price declines. Thus, the 20-30% annual decline in manufacturing cost associated with Moore's Law could be interpreted as a floor on the quality-adjusted price declines in the most competitive segments of the semiconductor market.

2. Other Benefits from "Moore's Law" Manufacturing Innovation

Impressive declines in transistor manufacturing cost, accompanying denser chips with smaller feature sizes at more advanced technology nodes, measure only a part of the economic benefits of the Moore's Law innovation dynamic. With smaller transistor sizes also came faster switching times and

[24] At SEMATECH, the US semiconductor industry consortium (with which the author worked as a consultant in the first decade of the 2000's), the planning rule of thumb was that a fab would be a candidate for an upgrade to a new technology node no more than twice over its lifetime, and then would be shut down as uneconomic.

lower power requirements.[25] The complementary benefits of speed and power improvements were highly significant for chip consumers (like computer makers) and their customers.

This was particularly true for chip makers manufacturing microprocessors. Existing computer architectures running at faster speeds run existing software faster and enable more data processing in any given time. Until 2004, computer processor clock rates increased rapidly, as did performance of computers incorporating these faster microprocessors. Figure 4 shows clock rates for Intel desktop microprocessors in computers tested on industry standard benchmark programs over the last twenty years, as well as benchmark scores for these computers. As clock rates increased, so did performance.[26] Cheaper processors were also faster—stimulating increased demand for new computers in offices, homes, and workplaces.

Log (Processor Speed) *Log(Performance)*

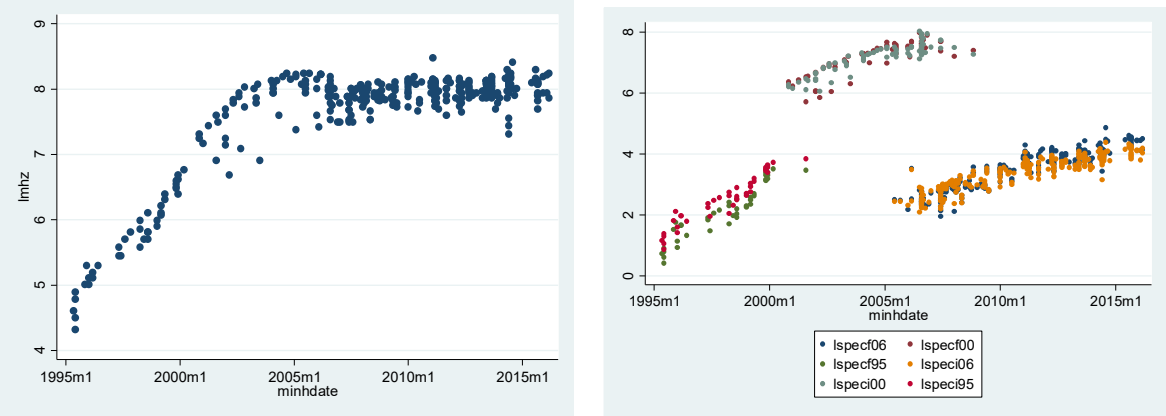


Figure 4. Processor clock rate and performance for Intel desktop processors running SPEC CPU benchmarks, by first availability date of tested hardware

Source: Author's analysis of SPEC submissions, SPEC.org. Performance scores for 1995, 2000, and 2006 SPEC benchmarks have different values for same processor, and different vintage benchmark scores are not directly comparable.

The logarithmic scale used in Figure 4 obscures a fairly dramatic slowdown in improvement in CPU performance after the millennium. Table 2 shows compound annual growth rates in performance over time of Intel desktop processors on standard CPU benchmark software (the SPEC benchmarks). (See Appendix A1.)

Three different versions of the SPEC CPU test suite were released—one around 1995, one in 2000, and the most recent in 2006. Each suite contains a selection of "integer" application tests (e.g., programming and code processing, artificial intelligence, discrete-event simulation and optimization,

[25] The underlying theory ("Dennard scaling") suggested that a 30% reduction in transistor length and 50% reduction in transistor area would be accompanied by a 30% reduction in delay (40% increase in clock frequency), and 50% reduction in power. Esmaeilzadeh, et.al., (2013), p. 95.

[26] For given software and computer architecture, time required for programs to execute is inversely proportional to processor clock rate, assuming data transfer does not constrain performance. Lower rates of performance improvement after 2004, as processor clock rates plateaued, were obvious to computer designers. See Fuller and Millett (2011), chap. 2; Hennessey and Patterson (2012), chap. 1.

gene sequence search, video compression), and a set of "floating point" math-intensive application tests (e.g., solution of systems modeling problems in physics, fluid dynamics, chemistry, and biology, finite element analysis, linear programming, ray tracing, weather prediction, speech recognition). These test suites are designed to test single process (programming task) performance on a CPU.[27]

In addition, so-called "rate" versions of these test suites, which run multiple versions of the single process benchmarks simultaneously on a single CPU, are available. The "rate" benchmarks are intended to show how the CPU would perform as a server running multiple independent jobs, or alternatively, running an "embarrassingly parallel" programming problem—a task which could be divided up into multiple software processes not requiring any communication or coordination between processes.[28]

Changes in trends over time in the SPEC benchmark performance scores for Intel desktop processors are quite dramatic.[29] Over the 1995-2000 period, integer computing performance increased by about 58 percent annually, floating point performance by 64%. The suite was revised in 2000, and from the end of 2000 through 2004, both integer and floating point performance improvement rates were almost halved, to an increase of about 33-34% per year.[30] Finally, over the most recent time period, after the 2006 revision of the SPEC benchmarks, from 2005 through 2016, annual performance gains were reduced substantially again, to rates of 17% (integer) and 25% (floating point) annual improvement.[31]

[27] The overall benchmark score is calculated as a geometric mean of scores on the individual programs within the benchmark.

[28] Unfortunately, there is no SPEC rule about how many instances of the single benchmark programs should be run for the rate benchmarks on a multicore CPU. It could be as many as the number of cores in the CPU, or twice that number (the number of threads that can be run simultaneously on a CPU with additional processor hardware supporting symmetric multi-threading—a feature called hyperthreading by Intel), or some number of instances less than either of those bounds.

[29] Pillai analyzed the apparent slowdown in microprocessor quality improvement (as measured by software benchmarks) from 2001-2008. See Pillai (2013), Figure 1.

[30] There was a statistically significant—but substantively insignificant—additional decline of under a percent per year after 2004, through 2007.

[31] There was another statistically significant, but substantively insignificant, decline by a fraction of a percent in performance improvement rates after 2012.

SPEC CPU Benchmark	Coef. CAGR	Robust Std. Err.
1995m5-2000m3		
int95	.5826577	.0175146
fp95	.6397016	.0231907
int95_rate	.6241582	.0273672
fp95_rate	.7227752	.0331
2000m11-2004m11		
int2000	.3304092	.0173773
fp2000	.3429411	.023522
int2000_rate	.4697731	.0512966
fp2000_rate	.3989549	.0351676
2005m2-2007m1		
int2000	.3222474	.016442
fp2000	.3365855	.022279
int2000_rate	.4650892	.0475414
fp2000_rate	.3986346	.032545
2005m6-2012m11		
int2006	.1709304	.0069587
fp2006	.2467286	.0077563
int2006_rate	.2472256	.013015
fp2006_rate	.2537211	.0101781
2013m1-2016m5		
int2006	.1687175	.0064265
fp2006	.2414989	.0070952
int2006_rate	.2417978	.0119286
fp2006_rate	.2480768	.0093352

Table 2. Annual growth in processor performance improvement over different time periods and benchmarks
Source: Author analysis of SPEC benchmark performance of Intel desktop processors.

3. An End To Moore's Law?

Unfortunately, the golden age of more rapidly cheapening transistors (which were also faster and drew less power) that began in the late 1990s did not survive unchallenged past the new millennium.

2004: the end of faster. The first casualty was the "faster thrown in for free," along with smaller, cheaper, and greener. Around 2003-2004, higher clock rates stalled (see Figure 4), as disproportionately greater power was required to run processors reliably at ever higher frequencies. With tinier transistors running at higher power in denser chips, dissipating heat generated by higher power density became impossible without expensive cooling systems. (The highest processor speed shipped by Intel until very recently was 4 GHz; IBM's fastest z-series mainframe CPU, with advanced cooling, hit 5.5 GHz in 2012, but subsequent CPUs ran at lower frequencies.[32]) Intel and others abandoned architectures reliant on frequency scaling to achieve better processor performance after 2004. Clock rates in subsequent processor architectures actually fell and processing more instructions per clock tick became the focus for improved computing performance.

Two-year node introductions continued to produce smaller and cheaper transistors, though. Ever cheaper transistors were utilized to create more CPUs—"cores"—per chip, thus processing more

[32] Raley (2015), p. 23.

instructions per clock at lower clock frequencies. This new "multicore" strategy's weakness was that application software required "parallelization" to run on multiple cores simultaneously, and software applications vary greatly in the extent to which they can be easily parallelized. Further, improving software was more costly than simply adopting the cheaper hardware delivered by new technology nodes: quality-adjusted prices for software historically have fallen much more slowly than quality-adjusted prices for processors.[33]

The difficulty and cost of parallelization of software is an economic factor limiting utilization of cheap multicore CPUs on hard-to-parallelize applications.[34] In addition, a fundamental result in computer architecture (Amdahl's Law) maintains that if there is any part of a computation that cannot be parallelized, then there will be diminishing returns to adding more processors to the task—and in many applications, decreasing returns are noticeable fairly quickly. One widely used computer architecture textbook summarized the challenges in utilizing multicore processors: "Given the slow progress on parallel software in the past 30-plus years, it is likely that exploiting thread-level parallelism broadly will remain challenging for years to come."[35]

2012: the end of rapid cost declines? Until roughly 2012, transistor fabrication costs continued falling at rapid rates. At the 22/20nm technology node, which went into volume production around 2012 (at Intel), continuing cost declines began to look uncertain. Figure 5 shows contract chipmaker GlobalFoundries' 2015 transistor manufacturing costs at recent technology nodes.[36]

Numerous fabless chip design companies, which outsource chip production to contract manufacturing "foundries," began to publicly complain that transistor manufacturing costs had actually *increased* at the 20/22nm node.[37] (Fabless companies accounted for 25% of world semiconductor sales in 2015; foundries, which also build outsourced designs for semiconductor companies with fabs, had a 32% share of global production capacity.[38]) Charts like Figure 6, showing increased costs at sub-28nm technology nodes, were frequently published between 2012 and 2016. Figure 6 is not inconsistent with

[33] Economic studies of mass market, high volume packaged software prices have typically found quality adjusted rates of annual price decline in the 6 to 20 percent range. See for example, Neil Gandal, "Hedonic Price Indexes for Spreadsheets and an Empirical Test for Network Externalities," *RAND Journal of Economics*, Vol. 25, No. 1 (Spring, 1994); S. Oliner and D. Sichel, "Computers and Output Growth Revisited: How Big Is the Puzzle?", *Brookings Papers on Economic Activity*, Vol. 25, No. 2, 1994; A. White, J. Abel, E. Berndt, and C. Monroe, "Hedonic Price Indexes for Personal Computer Operating Systems and Productivity Suites," *Annales D'Economie et de Statistique*, No. 79/80 (2005), A. Copeland, "Seasonality, Consumer Heterogeneity and Price Indexes: The Case of Prepackaged Software," *Journal of Productivity Analysis*, vol. 39, no. 1, (2013), M. Prudhomme and K. Yu, "A Price Index for Computer Software Using Scanner Data," *Canadian Journal of Economics*, vol. 38, no. 3 (2005).

[34] The opposite--software problems easily divided up across processors and run with little or no inter-processor communication or management required—are described in the computer engineering literature as "embarrassingly parallel".

[35] Hennessey and Patterson (2012), p. 411.

[36] Like Table 1, this figure probably does not include R&D costs.

[37] Fabless chipmakers Nvidia, AMD, Qualcomm, and Broadcom all publicly complained about a slowdown or even halt to historical decline rates in their manufacturing costs at foundries. Shuler(2015), Or-Bach (2012), (2014), Hruska (2012), Lawson (2013), Qualcomm (2014), Jones (2014), (2015).

[38] Foundry share calculations based on Yinug (2016), Rosso (2016), IC Insights (2016). Charts like Figure 4 should be viewed cautiously, as underlying assumptions about products, volumes, and costs are rarely spelled out in published sources.

Figure 5, since Figure 6 likely includes the fabless customer's non-recurring fixed costs for designing a chip and making a set of photolithographic masks used in fabrication, while Figure 5—the foundry's processing costs—would not.[39] These fixed costs have grown exponentially at recent technology nodes and create enormous economies of scale.[40] Some foundries have publicly acknowledged that recent technology nodes now deliver higher density or performance at the expense of higher cost per transistor.[41]

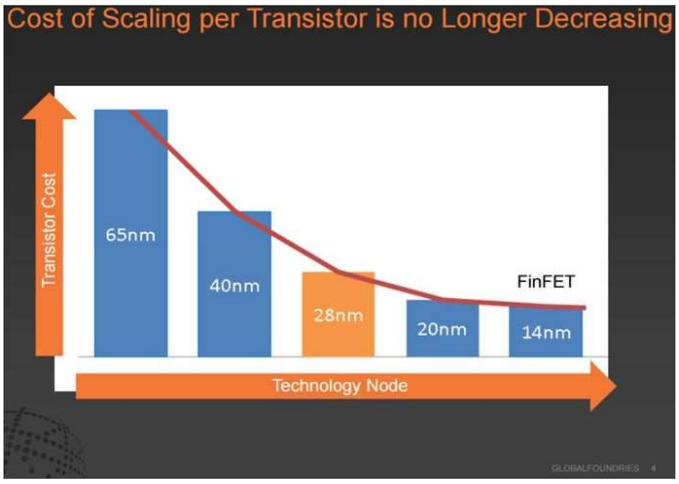
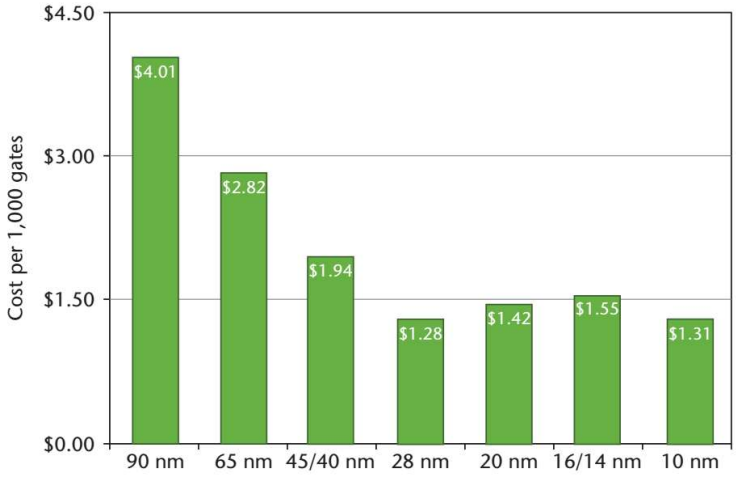


Figure 5. Global Foundries' transistor manufacturing cost at recent technology nodes
Source: McCann (2015).



[39] Historically, a set of 10 to 30 different photomasks was typically employed in manufacturing a chip design. For a low to moderate volume product, acquisition of a mask set is effectively a fixed cost.

[40] Brown and Linden (2009), chap. 3. McCann (2015) cites a Gartner study showing design costs for an advanced system chip design rising from under $30 million at the 90nm node in 2004, to $170 million at 32/28nm in 2010, to $270 million at the 16/14nm node in 2014.

[41] Samsung's director of foundry marketing: "The cost per transistor has increased in 14nm FinFETs and will continue to do so." Lipsky (2015). "GlobalFoundries believes the 10nm node will be a disappointing repeat of 20nm, so it will skip directly to a 7nm FinFET node that offers better density and performance compared with 14nm." Kanter (2016).

Figure 6. Cost per logic gate, with projection for 10nm technology node
Source: Jones (2015)

Because of these trends, fabless graphics chip specialists Nvidia and AMD actually skipped the 20/22nm technology node, waiting a high-tech eternity—five years—after launch of 28nm graphics processors in 2011 to move to a new technology node (14/16nm) for their 2016 products.

2018: "dark silicon" and limits on green? The microprocessor industry's response to the end of frequency scaling was to use ever cheaper transistors to build more cores on a chip. Though limited by software advances in parallelizing different kinds of applications, this strategy at first seemed effective. More recently, continued future improvement of CPU performance on even easy-to-parallelize applications has been questioned.

As transistors get very small, power requirements to switch these transistors are not reduced at the same rate as transistor size. The "green" lower power benefit of smaller transistors diminishes. Furthermore, as the power density of chips increases, heat dissipation becomes an issue. Thus, the heat problem that blocked further frequency scaling returns in a new guise and prevents the increasing numbers of smaller cores squeezed into a multicore chip from simultaneously operating at a chip's fastest feasible clock rate.

The fraction of a chip's cores that must be powered off at all times in order for a chip to operate within thermal limits, dubbed "dark silicon" by researchers modeling the problem, had been projected to grow as large as 50% by 2018.[42] Indeed, current PC users are already seeing their multicore machines "throttling" with attempts to use all cores for intensive computations at the highest clock rates, hitting thermal limits and then either falling back to lower clock rates, or idling cores. Continued reductions in power requirements are still feasible, but no longer are a free benefit of Moore's Law—they now come at the cost of reduced speed, and additional on-chip circuitry needed to turn off power to unused portions of a processor chip.

2021+: an end to smaller in conventional silicon? Even some manufacturing technologists from Intel now believe that the Moore's Law cadence of technology nodes, with ever smaller feature sizes in conventional silicon, will end sometime in the next five years. Intel's Bill Holt put it in these terms recently:

> "… Intel doesn't yet know which new chip technology it will adopt, even though it will have to come into service in four or five years. He did point to two possible candidates: devices known as tunneling transistors and a technology called spintronics. Both would require big changes in how chips are designed and manufactured, and would likely be used alongside silicon transistors."[43]

Can We See A Slowing Down of Moore's Law Cost Declines in Price Statistics?

[42] Esmaeilzadeh, et. al. (2013), pp. 93-4.
[43] Bourzac, (2016).

If Moore's Law has slowed or even stopped, we would expect to see it in economic metrics, like prices and manufacturing costs.[44]

Prices

An obvious place to look is in the price statistics for computer memory chips, which remained the mass volume semiconductor product par excellence through the end of the 20th century. DRAMs were later superseded by flash memory as the technology driver for new memory manufacturing technology. After the millennium, new technology nodes were first adopted in flash memory chips before DRAMs; flash had become the highest volume commodity chip by sales around 2012.[45]

Table 3 shows changes in price indexes for high volume memory chips. The DRAM "composite" index is a matched model, chain-weighted price index based on consulting firm Dataquest's quarterly average global sales price for different density (bits per chip) DRAM components available in the market over the years 1974-1999.[46] This data has no longer been available in recent years.

		Compound Annual Decline Rate					
		Flamm-Aizcorbe DRAM Composite	BoK $EPI DRAM	BoK $EPI Flash	BoK DRAM PPI	BoK Flash PPI	BoJ Chain-Wtd MOS Mem PPI
1974:1-1980:1		-45.51					
1980:1-1985:1		-43.45					
1985:1-1990:1		-24.74					
1990:1-1995:1		-17.40	-10.81				
1995:1-1999:4		-46.37	-44.28		-33.26		
1999:4-2005:1			-28.94	-31.28	-31.76		-24.04
2005:1-2011:4			-37.94	-26.92	-30.65	-29.28	-28.79
2011:4-2016:4			2.33	-12.70	-1.42	-5.76	-13.57

Table 3. Price indexes for memory chips

In the mid-1980s, Korean producers Samsung and Hynix entered the DRAM business, and, along with US producer Micron Technology, now account for the vast bulk of current DRAM sales.[47] The Bank of Korea's export price index (based on dollar basis contracts) and the Bank of Korea's producer price

[44] A very useful bibliography of prior matched model and hedonic studies of semiconductor prices may be found in Aizcorbe (2014), pp. 107-108.

[45] See http://www.icinsights.com/news/bulletins/Total-Flash-Memory-Market-Will-Surpass-DRAM-For-First-Time-In-2012/ .

[46] The data prior to 1990 is the same data used in Flamm (1995), Figure 5-2. From 1990 on, the data are taken from Aizcorbe (2002).

[47] Taiwanese firms entered the DRAM market in force in the early 1990s, but have since largely exited, as have all Japanese producers (US producer Micron acquired Japanese DRAM fab facilities). The last remaining European producer (Qimonda) filed for bankruptcy in early 2009. By 2011, the top 3 producers (Samsung, Hynix, and Micron) accounted for between 80 and 90% of global sales. See Competition Commission of Singapore (2013).

index (PPI, converted to a dollar basis using quarterly average exchange rates) for DRAM and flash memory chips are available.[48]

Finally, since 2000, the Bank of Japan has published a chain-weighted "MOS memory PPI" with weights that are updated annually. This index is likely to be predominantly a mix of DRAM and flash memory, tilting more toward flash in recent years. Generally, except for the period from 1985-1995, when a string of trade disputes (between the US and Europe, and Japanese, Korean, and Taiwanese memory chip producers) had significant impacts on global chip prices,[49] prices for DRAMs and flash fell at average rates exceeding 20-30% annually.

It is notable that rates of decline in memory chip prices in the last five years generally have been half or less of their historical decline rates over the previous decades. Korean price indexes (which track the majority of the DRAM manufactured and sold) have basically been flat for the last five years. US memory chip manufacturer Micron (like other flash memory manufacturers) is no longer planning to invest in new technology nodes beyond 16nm in its leading edge flash memory production. Instead, a new device design built vertically (3-D NAND) using existing manufacturing process technology is more cost effective than the continued planar scaling of components at new technology nodes described by the Moore's Law dynamic.[50] In DRAM, the mantra that "technology-driven growth slows due to scaling limits" ("scaling limits" being industry jargon for a slowing or ending of Moore's Law manufacturing cost reductions) had become a staple in Micron's investor conferences.[51]

Another "commodity-like" price in the semiconductor industry in recent years has been the cost that chip design houses face in having their chips manufactured on their behalf at so-called "foundries". The outsourced manufacturing of semiconductors designed at "fabless" semiconductor companies at foundries accounted for about 25% of world semiconductor sales in 2015. Foundries, which also build outsourced designs for semiconductor companies with fabs, held 32% of global production capacity in that year.[52]

A recent study of quality-adjusted fabricated wafer prices (the form in which manufactured chips are sold to the semiconductor design houses that have outsourced their production) by Byrne, Kovak, and Michaels (2017) portrays a slowing decline in fabricated wafer prices prior to 2012. (See Table 4.) While the pattern seems consistent with a slowing down of Moore's Law prior to 2012, this

[48] These are not well documented, but are believed to be fixed weight Laspeyres indexes, with weights updated every five years, that have been spliced together (2010 is the current base year). The export indexes are actually measured in dollars, while the Korean won-denominated and Japanese yen-denominated producer price indexes have been converted to dollars at current exchange rates. As a practical matter, except for a brief period during the 1980s when export controls related to the US-Japan Semiconductor Trade Agreement were put in place, DRAM prices historically and through the present have been set and quoted in dollars in a highly integrated global market. See Flamm (1993), pp. 163-4, 167-8. Flamm (1995), chapter 5, analyzes empirical evidence that regional price differentials in DRAM briefly appeared and then disappeared when restrictive trade policies were applied and then removed in the 1980s. With minuscule transport costs relative to product value, zero tariff costs globally for most countries (under the Information Technology Agreement, concluded in 1996, and bound into the WTO), and a large number of active global distributor/broker arbitrageurs, the global DRAM market has always been the poster child for the relevance of a "law of one price".

[49] See Flamm (1995).

[50] Micron 2015 Winter Analyst Conference (2015).

[51] Micron's Raymond James Institutional Investor Conference (2016); Micron Analyst Conference (February, 2017).

[52] Foundry share calculations based on Yinug (2016), Rosso (2016), IC Insights (2016).

study unfortunately ends with data from 2010, and thus cannot be used as a check against the claims of the most vocal US fabless designers (see above) that the prices they pay for having their transistors manufactured in foundries were no longer declining significantly at new technology nodes post-2012.

	Annual Index	% Rate of Change
2004	100	
2005	83.89521	-16.1048
2006	74.75891	-10.8901
2007	65.93704	-11.8004
2008	57.89118	-12.2023
2009	52.95437	-8.52774
2010	48.67003	-8.09062

Table 4. A quality-adjusted price index for fabricated "foundry" wafers

Source: Byrne, Kovak, and Michaels (2017).

Price Indexes for Intel Processors. Since their invention in the 1970s, microprocessor sales have grown rapidly, and since the 1980s have constituted another huge market segment. Official government statistics show a tremendous slowdown in the rate at which microprocessor prices have been falling after the millenium, as well as a significant attenuation in the rate at which prices of the desktop and laptop PCs that make use of these processors have declined. The U.S. Producer Price Indexes for microprocessors show annual (January-to-January) changes in microprocessor prices steadily falling from 60-70 percent peak rates during the "golden age" of the late 1990s and early 2000s, to a low of about one percent annual decline for the year ending in January 2015. (The Bureau of Labor Statistics stopped reporting its PPI for microprocessors in April 2015, apparently because of confidentiality concerns.) A parallel fall in price declines for laptop and desktop computers seems also to have occurred, from peak annual decline rates of 40%, in the late 1990s, to rates mainly in the 10-20% range in the last few years.

Table 5 shows compound annual decline rates in the PPI for microprocessors (including microcontrollers) as constructed by BLS, along with similarly defined indexes for the commodity "microprocessors". Annual decline rates slow from a rate near 50% in the late 1990s and first half decade of the new millennium, to a little over 10% in the second half of that first decade, to about 3% annually in recent years. This too is consistent with a substantial slowing down in the impact of Moore's Law manufacturing technology innovation.

The Bureau of Labor Statistics had historically been somewhat opaque about its methodology in constructing its microprocessor price series (there is no published methodology describing precisely how these numbers were constructed).[53] It is believed that these were matched model indexes based on some weighted selection of products appearing on Intel list price sheets (the same data source I utilize below),[54] but this is not entirely certain. There is also some evidence that the BLS may have

[53] Ironically, the BLS is now much more open about the details of how it constructs the current (unpublished) microprocessor price index than it was about some previous (published) versions. See Sawyer and So (2017).
[54] Based on a brief conversation with BLS officials, Cambridge, MA, July 2014. See also Sawyer and So (2017).

experimented with several different methodologies for measuring its microprocessor price indexes over the 1995-2014 periods,[55] before ceasing publication of the index for confidentiality reasons in 2015.

		Microprocessors (including microcontrollers)			
		Commodity Price		Producer Price	
		Index (discont)	Index (current)	Index	
1995:1-1999:4		-50.0		-50.5	
1999:4-2004:4		-48.6		-49.2	
1999:4-2005:1				-47.8	
2005:1-2007:4				-37.7	
2007:4-2011:4			-10.8	-10.8	
2011:4-2015:1			-3.0	-3.0	

Table 5. Annualized decline rates for microprocessors per the BLS
Author's calculation. Middle month for quarter used, except Dec. 2007 used for 2007:4.

As an alternative to the BLS measure, I have previously constructed alternative price indexes for Intel desktop microprocessors, tracing the contours of change over time in microprocessor prices using a unique, highly detailed data set I have collected over the last two decades.[56] Since the mid-1990s, Intel has periodically published, or posted on the web, current list prices for its microprocessor product line, in 1000-unit trays. These list prices are available at a very disaggregated level of detail, distinguished between similar models manufactured with different packaging, for example, and were typically updated every 4 to 8 weeks—though price updates have sometimes come at much shorter or longer intervals.[57] By combining these detailed prices with detailed attributes of different processor models, it is possible to construct a very rich data set relating processor prices to processor characteristics, over time.

This permits the construction of both "matched model" price indexes, the traditional means by which government statistical agencies measure industrial prices, and so-called "hedonic" price indexes,

[55] The BLS web site showed three different "commodity" price indexes (as opposed to its single microprocessor producer price index) for microprocessors over this period. The most recent microprocessor "commodity" price index is based in December 2007, but is only reported on a monthly basis from September 2009 through 2015. There are also two discontinued microprocessor commodity price indexes, one based in December 2004, and running through June 2005, and another based in December 2000 and running from 1995 through December 2004. One might speculate that the BLS changed its methodology for measuring microprocessor prices three times during this period.
[56] See Flamm (2007).
[57] My data initially (over the 1995-1998 period) made use of compilations of this data collected by others and posted on the web; since 1998-99, most of this data was collected and archived directly off the Intel web site.

which relate processor prices to processor characteristics. It is now well understood in the price index literature that there is a close relationship between matched model indexes and hedonic price indexes.

The Intel dataset permits measuring differences in processor characteristics down to individual models of processors, controlling for such things as processor speed, clock multiplier, bus speed, differing amounts of level 1 ("L1"), level 2 ("L2"), and level 3 ("L3") cache memory, architectural changes, and particular new processor features and instructions. The latter have become particularly important recently—beginning in mid-2004, Intel dropped processor clock speed as the principle characteristic used to differentiate processors in its marketing and introduced more complex "processor model number" systems that distinguish between very small and arguably minor differences between processors that proliferated at more recent product introductions.

For comparison purposes, I begin by constructing a matched model price index for Intel desktop processors. Since I do not have sales or shipment data at the individual processor model level, I weight each observed model equally, by taking the geometric mean of price relatives for adjoining periods in which the models are observed.[58] A price index based on the simple geometric mean of individual product price relatives (dubbed the Jevons price index), is chained across pairs of adjacent time periods, and depicted in Figure 8. It has the same qualitative behavior as the official government producer price index for microprocessors, falling at rates exceeding 60% in the late 1990s, and slowing to a decline rate under 10% since 2009.

This geometric mean matched model index actually falls a little more slowly than the official U.S. microprocessor PPI, which may be attributable to the fact that the geometric mean index weights all models equally, while the PPI probably uses a subset of the data, with some weighting scheme for models drawn (and replaced periodically) from subsets of processor types. The PPI also uses fixed weights from some base period to weight these price changes, while my Jevons index chains adjoining paired comparisons of models, and therefore implicitly allows weights given to different models over pairs of adjoining time periods to evolve over time.

I have also constructed a hedonic price index, using an econometric model which utilizes more of the information available in my sample of Intel list prices. The basic hedonic price model I estimated statistically was

$$\textbf{(H0)}\ lprice_{it} = constant + d_t + b_a\ arch\_d_i + b_p * lproc_i + b_m\ lmaxmhz_i + b_w\ lbw_i + b_{co}\ lcores_i + b_h\ ht_i + b_{ca}\ lcache_i + b_g\ int\_graph_i + b_{tdp}\ ltdp_i + b_{64}\ em64t_i + b_{st}\ eist_i + b_v\ vt_i + u_{it}$$

with the following covariates, for chip model i, period t:

d_t	a time dummy indicator variable for the later period in a pair of adjacent time periods
$arch\_d_i$	architecture dummy for Intel chip architecture (e.g., Haswell, Coppermine, Ivy Bridge)
$lproc_i$	log of base processor clock rate
lmaxmhz	log of maximum clock rate if processor has turbo mode, = lproc if not

[58] Since there occasionally were multiple price sheets issued within a single month, I have averaged prices by model by month. Since Intel did not issue new prices sheets on a monthly basis, "adjoining time periods" means temporally adjacent observations.

lbw_i	log of memory bandwidth (8 x memory bus clock rate if older front side bus architecture, or max memory bandwidth if reported in Intel Ark database)
$lcores_i$	log of number of physical cores on chip
ht_i	hyperthreading (additional virtual core per physical chip core) hardware support, binary indicator variable
$lcache_i$	log of maximum cache memory for highest level cache on processor
int_graph_i	binary indicator variable for integrated graphics, 1 if on chip graphics
$ltdp_i$	log of thermal design power (watts), rating of chip
$em64t_i$	binary indicator dummy for Intel 64-bit memory architecture
$eist_i$	binary indicator dummy for enhanced Intel speedstep technology (dynamic frequency scaling and power reduction) feature
vt_i	binary indicator dummy for hardware virtualization support, 1 if virtualization hardware support

and u_{it} a statistical disturbance term for chip model i, time period t.

Choice of Characteristics. Choice of characteristics was primarily based on a review of the computer architecture literature (discussed below). The most widely used textbook in that literature holds that computer instruction processing performance is based primarily on the ***processor architecture*** (which determines how many software instructions can be executed per processor clock cycle: ***IPC***, or instructions per clock) and the computer's ***clock rate***. Since the mid-2000s, desktop PC processors have further boosted performance by incorporating a ***turbo*** mode, increasing clock rate to some ***maximum*** above the chip's baseline frequency for short periods of time. Frequently, software performance can also depend its on-chip (***cache***) ***memory size***, and on the sustained speed at which a computer can transfer data from its off-chip, secondary memory—its ***maximum memory bandwidth***. Over the last decade, additional processor units (cores) have been added to desktop computer processors, and if software can be parallelized and run simultaneously on multiple ***cores***, this too will improve performance. In addition, adding hardware support for "virtual cores," so that a hardware processor core can be time-shared simultaneously by two instruction-processing threads, can speed things up—Intel's version of this feature is called ***hyperthreading***. Several other features—hardware support for ***virtualization***, a ***64-bit memory architecture***—can improve computer performance on particular applications, particularly when desktop processors are used in servers. Basic ***graphics*** are now integrated onto many processor chips, sparing the end user the need to purchase a costly discrete graphics card, which should also affect demand for a processor by consumers. Finally, power consumption is probably the major variable cost of computing (and drives use of relatively expensive cooling systems needed to dissipate heat from high-powered processors). Low thermal design power (***TDP***) in desktop processors is considered beneficial for this reason,[59] and processor makers like Intel have also developed hardware support for power-saving features in the chip's micro architecture (Intel's proprietary version—enhanced Intel Speedstep—is abbreviated ***EIST***).

Note that maximum memory bandwidth, cache sizes, numbers of cores, and even TDP typically take on only a handful of discrete values in any two-period estimation sample interval, and are often perfectly collinear with binary indicators for processor architecture, 64-bit support, hardware virtualization, and integrated graphics. In addition, as I show below, performance on different SPEC

[59] In addition, low power consumption has the additional very important benefit of producing longer battery life in a laptop computer, irrelevant for a battery-less desktop computer processor.

processor benchmark suites is nearly perfectly predicted by a linear combination of a subset of five of these processor characteristics (chip architecture, clock rate, number cores, hyperthreading, turbo mode).

The regression coefficients (weights) on each of these characteristics, however, vary substantially by software benchmark type. Since the mix of software programs run on computers has evolved substantially over time (these changes have led SPEC to periodically revise its various benchmarks), using the underlying characteristics determining processor benchmark performance (rather than a particular benchmark score) seems the more flexible way to accommodate the impact of changes over time in market demand for different types of software applications running on computers.

The very same characteristics that one might expect to affect processor demand, would also be expected to affect processor cost, on the supply side. Faster chips supporting the highest clock rates are culled from larger numbers of chips fabricated in batches of wafers, through extensive testing (a process dubbed "binning" within the industry). Slower- and faster-running chips are are sorted into higher and lower performance bins and and sold as distinct chip models. Processors with defects in circuitry in their memory caches and feature circuits, too, have their defective circuitry fused off electronically and are then sold as lower performance chips (with less memory and features). Redundant circuits can be added to a chip design (at a cost, by increasing chip die area) to yield larger shares of chips on a wafer with functioning features. Every desirable feature of a processor also has some incremental cost incurred in order to increase the number of chips produced with that functioning feature—either through a bigger and therefore more costly chip footprint on a silicon wafer (driven by redundant circuitry needed to fix defects), or through the larger numbers of wafers that must be processed in order to get the desired target numbers of chips with functional features and characteristics.

Computer architectures also affect processor cost, as well as performance, since numbers of transistors on a chip, and therefore chip manufacturing cost, are directly related to the chip's architecture. In addition, since at least the early 2000s, Intel has marked the introduction of new manufacturing technology nodes by rolling out improved chip architectural designs when introducing the new node. So manufacturing technology nodes and chip architectural family will be perfectly collinear in a statistical analysis of Intel prices and costs.

In short, the chip characteristics in this hedonic regression would be expected to affect both computing performance and power consumption, as well as processor cost, and are relevant to both the demand and supply cost sides of the market. For that reason, even if a single, perfectly accurate measure of average processor computing performance (a "market average" benchmark based on the relative mix of software applications run by final computer end users in computing service markets at that particular moment in time) existed, changing in perfect lockstep with the changing mix of applications run by different end users,[60] changes in processor characteristics would have additional impacts on price working through processor manufacturing cost, and therefore need to be accounted for separately in the estimated hedonic price equation.

[60] It is worth noting that the SPEC benchmarks report an unweighted geometric mean of performance in a variety of applications, and that these fixed (equal) weights remain fixed over long periods of time (since 2006, as of October 2018) for the SPEC benchmark composite scores.

One potentially important pitfall in using large numbers of characteristics in a hedonic equation is that many of these characteristics are likely to be perfectly collinear with others. This is a real world problem. For example, all the chips developed with a new architecture design may, at least initially, have a common size for their highest level cache, or may all have a 64-bit architecture, or may all have hyperthreading. Most regression software will drop perfectly collinear characteristics automatically, and the coefficients of the other covariates (the ones with which the dropped characteristics are perfectly collinear) will include the effects of the dropped covariates in their estimated values.

This can make interpretation of signs and values of hedonic characteristics problematic, and liable to big jumps in value (and coefficient interpretation) in different estimation periods, depending on which characteristics are perfectly collinear, and which characteristics are dropped (often automatically) by the statistical software. It also may appear at first glance to look like undesirable "coefficient instability".

However, as long as the key variable of substantive interest (the last period time dummy variable in a regression model spanning two adjacent time periods, the coefficient of which is used to construct a hedonic price index) is not perfect collinear with the other included characteristics variables, there is no difficulty in interpreting the coefficient of the time dummy variable. Fortunately, it is straightforward to check that this is the case, by simply running an auxiliary linear regression of the time dummy on all other explanatory covariates and verifying that it is not perfectly predicted by other regression covariates.

Perfect collinearity in a simple hedonic simulation. The problem of perfect collinearity—and its effects—is very real in my sample of Intel microprocessors. In every single pair of adjacent time periods multiple characteristics are dropped as perfectly collinear by statistical software. The problems this can create in interpreting regression results is easily illustrated in a simple simulation model.

Consider a simplified, stylized processor market over two adjacent time periods. Suppose half of manufacturing capacity is used to fabricate a baseline processor architecture (arch_dummy=0), and half dedicated to a different architectural alternative (arch_dummy=1). Suppose that initially, half of fabricated chips from both architectures can run at clock rate of 1000, and half at 1500. All chips manufactured run 500 faster in the later period (i.e., half at 1500, half at 2000 (think of this as the result of manufacturing process improvement). Substantively, this means there will be a positive correlation between a binary time period indicator variable (first_period=0, last_period = 1) and processor clock rates.

Let us also suppose that the only thing all processor buyers care about is processing speed on a single, common software application (so we are ignoring the problem of heterogeneity in demand—i.e., which benchmark to run). Further, let's assume that this single measure of speed (software processing performance) relevant to users is perfectly determined by a simple linear function of three processor characteristics—

*speed = clock_rate + 500*arch_dummy + 200*turbo*

(where 'turbo' is a binary indicator for a functioning turbo speedup feature that is enabled in half of the chips produced for each architecture and clock combination).

Each unique combination of architecture, clock rate, and turbo capability under these assumptions can be thought of as a distinct "processor model".[61] With this setup, there are twelve distinct microprocessor models (2 processor architectures x 3 clock rates x 2 turbo values), sold over two periods. Half the models are sold in both periods (the ones running at 1500), and half sold only in the beginning or end periods (the models running at the 1000 and 2000 clock rates, respectively).[62]

Unit manufacturing cost for the chip is assumed to be given by

*cost = 50 + 2 * clock_rate + 2000 * turbo + 500 * arch_dummy –10 * end_period.*

End-period manufacturing costs decline by $10 for any constant quality "computer model," simulating a uniform $10 drop in manufacturing cost, given any set of fixed model characteristics, over time.

In the spirit of Pakes (2003), we write out an extremely simple hedonic price reduced-form equation

*price = 600 + 2 * speed + cost + random disturbance term*,

with the first two terms on the right hand side of the equation reflecting the further assumption that expected markup over incremental unit cost, reflecting user demand, is a linear function of speed alone. After substituting for unit cost (which we typically cannot observe in available data), this gives us a "hedonic price equation" as a function only of observable processor characteristics:

(H1) *price = 650 + 2 *speed + 2 * clock_rate + 2000 turbo + 500 * arch_dummy – 10 * end_period*

+ random disturbance term

The disturbance term in the simulation is drawn from a zero mean uniform distribution. The assumed across-the-board $10 end-period average reduction in manufacturing cost, conditional on fixed processor characteristics, induces a $10 decline over time in quality-adjusted (constant characteristic) mean price, across all computer models (since markup by assumption depends only on speed, in turn a function of the other processor characteristics we are conditioning on).

Most importantly, we cannot actually estimate (H1), because speed, architecture, frequency, and turbo characteristics, as a group, are perfectly collinear with one another (since speed is a linear function of arch_dummy, clock_rate, and turbo). Since these three chip characteristics exactly determine speed, any three of these four variables exactly determines the value of the fourth. If we were to substitute for speed as a function of its three determinants, and so drop it from the hedonic price equation, we get

(H2) *price = 650 + 4 * clock_rate + 1500 * arch_dummy + 2400 * turbo -10 * end_period .*

[61] I draw a sample of a ten million observations, using pseudo-random draws from independent uniform distributions to create a simulated population of processor "models," uniformly and independently distributed over architecture, clock rate and turbo feature. Another set of independent, pseudo-random draws from a uniform distribution create a mean zero disturbance term added into the realized sales price on the left-hand side of the hedonic price equation.

[62] Because clock rates increase over time, a binary indicator variable for the end period is positively correlated with clock rate, but uncorrelated with either architecture or the turbo feature (which are independently and randomly assigned to wafers/chips prior to fabrication).

If we substitute for turbo in terms of the other three variables, we get

(H3) *price = 650 + 12 * speed - 8 * clock_rate - 4500 * arch_dummy - 10 * end_period.*

If we substitute for clock_rate in terms of the other three characteristics , we get

(H4) *price = 650 + 4 * speed -500 * arch_dummy + 1600 * turbo – 10 * end_period.*

And substituting for architecture,

(H5) *price =650 + 3 * speed + clock_rate + 1800 * turbo – 10 * end_period.*

Table 6 summarizes a simple simulation demonstrating that with a large simulated sample (ten million observations), a regression model with any of the four above specifications (H2-H5) recovers the above parameters correctly.[63] A key point of substantial practical relevance is that **all four of these estimable specifications are correct, and produce exactly the same estimate for the coefficient of the time dummy variable**, the parameter of greatest substantive interest**.** But, the coefficients of the perfectly collinear characteristics need to be interpreted differently in each case, as the joint effects of that characteristic plus the effects of the dropped, perfectly collinear characteristic. In fact there are wild swings in coefficient values (from 12 to 3 for speed, from 1600 to 2400 for turbo) and even sign (from 1500 to -4500 for arch_dummy) as different candidates from the set of perfectly collinear variables get dropped from the estimated regression specification.

This is important because with large numbers of characteristics in a hedonic regression, particularly with binary dummies, or nominally continuous covariates that in any given time frame take on only a fixed number of discrete values, perfect collinearity among characteristics is very common. Covariates are typically dropped from the regression automatically by the econometric software. If this is happening, and different subsets of the perfectly collinear covariates are used in two different time periods, then wild variation in coefficient estimates, rather than representing worrisome instability in (non-perfectly collinear) explanatory covariates selected and used in the estimated regression.

A second, even more important point, is that estimated coefficients for variables that are not in the set of perfectly collinear variables are not affected by which of the perfectly collinear variables is dropped. In this simulation, for example, the estimated effect of the time dummy—the variable of greatest substantive interest, since its coefficient would be used to estimate a hedonic price index—does not change in value at all as the excluded perfectly collinear variable changes. It is likely to be relatively rare and fairly obvious when a time dummy variable is perfectly collinear with other covariates. In any event, it is easy to verify that the time dummy variable is not perfectly collinear with other included variables by simply running auxiliary regressions of the time dummy against all other explanatory variables, both those included and those dropped as perfectly collinear.

Finally, there is an important specification issue illustrated by this simulation. If one uses speed as one of the explanatory covariates, it is also important to include the full, non-perfectly collinear subset of relevant characteristics affecting cost, even if speed entirely captures the impact of these characteristics from the user demand side. Table 6 demonstrates that when only speed and time are used as explanatory variables (last column in the table), bias from the omitted characteristics greatly

[63] Appendix A2 contains the short Stata program giving these simulation results.

confounds the coefficient estimate for the time dummy variable, incorrectly magnifying the drop of quality-adjusted price by a factor of 7.5! We return to this point below.

Table 6. Simulation of Perfectly Collinear Characteristics in Hedonic Price Equation

	(drop speed)	(drop turbo)	(drop clock)	(drop arch)	(speed only)
	p	p	p	p	p
time	-10.22***	-10.22***	-10.22***	-10.22***	-75.24***
	(0.258)	(0.258)	(0.258)	(0.258)	(0.677)
clock_rate	4.000***	-7.999***		1.000***	
	(0.000365)	(0.000983)		(0.000517)	
arch_dum	1500.0***	-4499.8***	-500.1***		
	(0.183)	(0.492)	(0.258)		
turbo	2399.9***		1599.9***	1799.9***	
	(0.183)		(0.197)	(0.197)	
speed		12.00***	4.000***	3.000***	4.130***
		(0.000913)	(0.000365)	(0.000365)	(0.000762)
_cons	650.0***	650.0***	650.0***	650.0***	992.5***
	(0.492)	(0.492)	(0.492)	(0.492)	(1.281)
N	10000000	10000000	10000000	10000000	10000000
R-sq	0.980	0.980	0.980	0.980	0.808

Standard errors in parentheses
* p<0.05, ** p<0.01, *** p<0.001
Stata code for this simulation in Appendix A2.

A hedonic price index for Intel desktop processors. Model (H0) above was run for each of 162 pairs of adjacent months in which I collected Intel's desktop processor list prices.[64] The first set of adjacent list prices are for January and February 1996. The last pair of adjacent price sheets is for June and July 2014.[65] Overall R^2 was uniformly high, and was not driven primarily by the inclusion of the

[64] The list prices refer to per chip prices, for processors packaged in quantity 1000 trays sold to original equipment manufacturers (OEMs). By adjacent month, I mean a month and the next month in which an updated list price was published. For example, if Intel issued a price sheet in January, March, April, August, and November of a year, there would be four adjacent month pairs: January-March, March-April, April-August, and August-November. Roughly ¾ of the monthly observation pairs were a month apart; the next most frequent value observed was two months; the largest time gap between adjacent price lists observed was four months. A hedonic model excluding TDP produced useful estimates for price relatives over 162 adjacent pairs of months. Results for a model with TDP are shown in the appendix tables based on an initial period ending in October 1998, but the problem of a large share of observations lacking a TDP measure does not really fade away until the pair of adjacent months ending in January 2000.

[65] The number of processors in early years was very small and characteristics extremely collinear; numbers of processor prices (with TDP) in adjacent month pairs more than doubles from under 15 to over 30 in late 1999, and estimated price relatives after that date are probably much more reliable. See Appendix Table A4 and A6 for details on numbers of observations in different adjacent month samples. Entry and exit of architecture and indicator variables from estimation period to period has been color coded in this table. After the first non-zero observation for an indicator variable occurs, blanks indicate the variable was dropped as perfectly collinear. In no case was the time dummy variable perfectly collinear with other covariates; this was checked with auxiliary regressions.

architectural dummy variables—these were treated as fixed effects, and I also report a "within" R^2 (after demeaning all variables by their group mean) which is also quite high. (See Appendix Tables A4 and A6.)

The time dummy variables in the above regression were then exponentiated and used to construct price index relatives for adjacent time period pairs.[66] The resulting price index relatives were then used to chain link these period-to-period indexes into a longer chained price index, shown in Appendix Table A3.

In addition, I report the values of other coefficients in the hedonic regression in Appendix Table A5 and A7, which shows how large qualitative jumps in coefficient values from estimation period-to-period often occur as nonzero values for new characteristics, indicators, or architecture variables enter and exit the sample, due to perfect collinearity. But there is often perfect collinearity even when there is no new architecture or indicator entering or exiting the sample—this may be seen in the many blank coefficient estimates that appear when architecture or other indicators, or even continuous covariates (which often take on only a handful of discrete values in any single estimation period) are dropped due to perfect collinearity.

The processor architecture family variables are treated as fixed effects and not reported. There were anywhere from 1 to 7 such architecture fixed effects, depending on the pairs of adjacent months used for estimation of the hedonic equation.

Note that nominal power consumption for a processor (TDP, thermal design power) was simply unavailable for most Intel processors released prior to late 1999. I therefore estimated two versions of a hedonic index, one with TDP as a characteristic, and one without. TDP is statistically significant when it is used, and therefore the hedonic price index including TDP is the preferred index from 2000 on (the small numbers of observations with TDP reported prior to late 1999 make these pre-2000 estimates less reliable). I have linked the post-2000 index with TDP, to the pre-2000 index without TDP, and show this in the final column of Table A1 as a composite "best effort" index. The TDP-inclusive and -exclusive indexes are virtually identical from 2000 through January 2005, departing significantly from one another only afterwards. Prior to 2000, the earlier the time period, the more limited the available data, and the less reliable the resulting estimate.

Figure 7 visualizes some of the estimation model summary statistics from Appendix Table A6 for the TDP variant of the price index (which is also the "composite" index over the period from 2000 on). The upper panel shows an overall R-squared that across estimation periods averaged .96, and ranged from .91 to .99 from 2000 on. "Within" R-squared (explained variance after demeaning all variables by architecture fixed effects group means) averaged .92 and ranged from .74 to .99. The lower panel, using a logarithmic scale, shows that anywhere from 1 to 7 processor architectures were being listed for sale as Intel desktop processors during two-month adjacent estimation periods over this time frame. The number of observations used in the individual hedonic regressions after 1999 ranged from 28 to 190,

[66] One half of the coefficient's squared standard error was added to the exponentiated coefficient, to produce an unbiased estimate of the price relative (the exponentiated coefficient's value). See the sources cited in Triplett (2006), p. 54, fn. 41, for details on the rationale for the correction. Sergio Correia's *reghdfe* Stata command was used to estimate the hedonic regressions, because it removes non-informative singleton observations for dummy variables from the regression, because it provides detailed reports on perfectly collinear variables, and because it also calculates a "within" R^2, i.e., explained variance of the dependent variable after demeaning all variables within fixed effect groups—in this case, the processor architecture indicator variables were treated as fixed effects.

averaging 82. The average number of processor models per architecture per month listed for sale during the post 1999 period ranged from 4.7 to 24.5, indicative of significant historical changes to Intel's product differentiation strategies in marketing desktop processors, over time.

Some important substantive points are supported by Figure 7. First, there is substantial variation over time in how important the processor design (architecture) dummy variables are in accounting for price variation. While the overall explained variation in price in these hedonic regressions remained uniformly high, within relatively narrow bounds (.91 to .99) throughout the sample period, the role of architectural dummies varied greatly over different sub-periods. "Within" R-squared measures how much of the variation in price around architecture-specific means is explained by other covariates. The "within" R-squared coincides exactly with "overall" R-squared in the special case of their being only one "architecture" fixed effect (i.e., a single common constant intercept). The difference between overall and within R-squared can therefore be interpreted qualitatively as a measure of how important controlling for the multiple intercept levels (the processor architecture fixed effects) are in a hedonic model explaining price variation.

Figure 7 shows that, at times, a substantial share of overall explained variation (as much as a difference of .10 to .20 between overall R-squared and within R-squared) was accounted for by the processor architecture effects prior to 2003, and from late 2006 through 2012. Processor architecture effects from 2013 on are more modest contributors to explaining price variation, but not nil.

As is suggested visually by Figure 7, within R-squared (measuring the role of non-architectural characteristics in explaining price variation) has a negative and statistically significant correlation with the number of different desktop processor architectures present on Intel price sheets.[67] Not surprisingly, perhaps, it appears that processor architectural variation is more important in explaining price during periods when Intel marketed a larger variety of processor architectural designs, and less important in periods with less architectural variation. Indeed, the two measures of R-squared are virtually identical from 2003 through 2005, the heyday of the Pentium 4 series and its "Netburst" design, when only one or two design families accounted for all Intel desktop processors listed on its price sheets (compared with 4 architectures in 2002, and as many as 7 architectures in late 2006).

[67] For the TDP-inclusive hedonic specification, for adjacent periods ending after December 2000, the correlation coefficient between within R-squared and number of processor architecture dummies used is -.53. We reject the hypothesis that it is equal to zero (p-value is .0000).

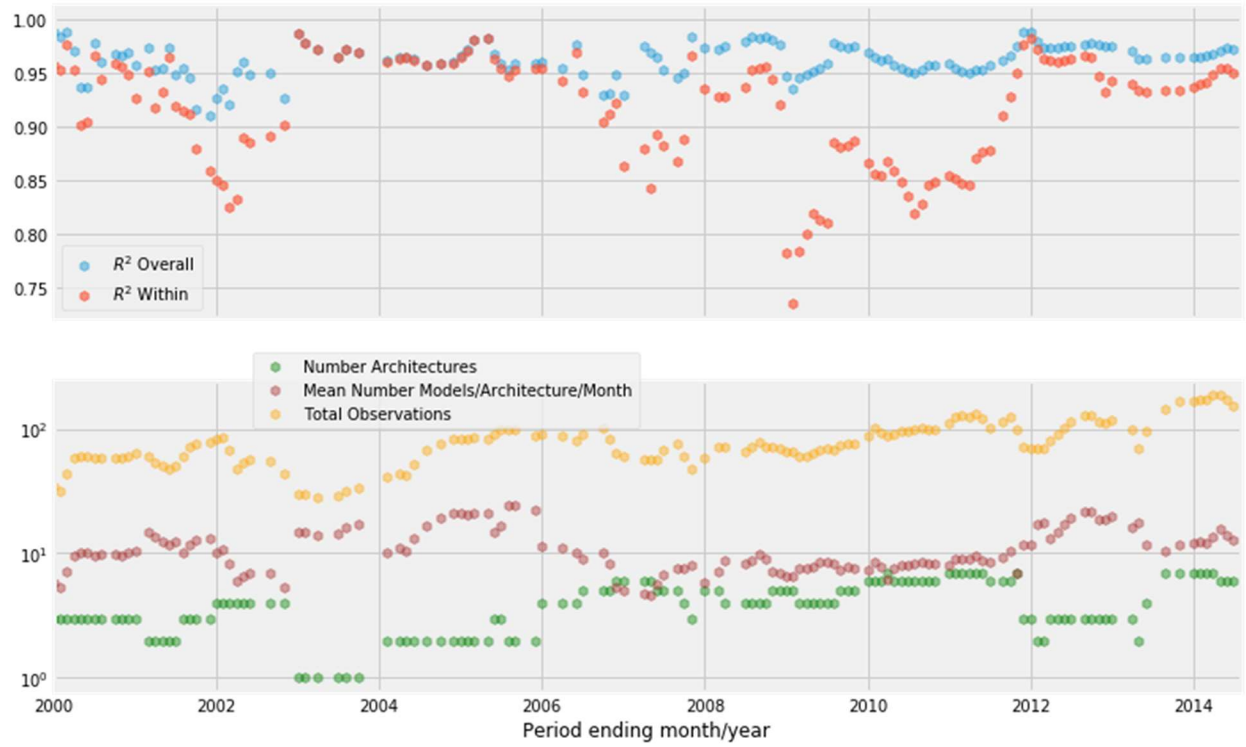


Figure 7 Summary Statistics for Hedonic Regressions
Source: Appendix Table A.6.

Figure 8 visualizes the hedonic price indexes produced using these models. A dramatic slowing of declines in quality-adjusted price from 2004 through 2006 is quite apparent, followed by a temporary resumption of a somewhat faster rate of decline after 2006, and then another marked slowdown from 2010 on.[68]

The first four columns in Table 7 compare my estimated hedonic and matched model price indexes and the BLS PPIs. As expected,[69] the matched model geometric mean (Jevons) index price declines are mostly very close to the hedonic indexes, but generally decline more slowly than those measured by the hedonic price index based on the same data set. My estimates over comparable earlier time periods are quite similar to the matched model indexes of Aizcorbe, Corrado, and Doms

[68] It is not coincidental that in 2004, the Pentium 4's architecture hit its clock rate ceiling, and power dissipation reached maximum limits compatible with inexpensive air cooling systems. The rollout of Intel's next generation response—the Conroe architecture (two cores on a single die, at a much lower clock rate, but more instructions per clock processed)—happened in mid-2006. To many industry observers, Intel appeared to be lagging behind its effectively duopolist rival AMD, architecturally, in the early 2000s. AMD was first to market with a 64-bit architecture, and later, the first single die dual core chip. (AMD had brought its Athlon X2 processor out in 2005, a full year before Intel's Core 2 Duo [Conroe architecture] chips.) For empirical evidence on AMD's technological challenge to Intel in the early 2000s, see Nosko (2011), Pakes (2017), European Commission (2009).

[69] Since if there were no entering or exiting processor models (all sampled processor models were observed in both time periods), and all hedonic coefficients were the same in the two adjacent periods (assumed by the time dummy method), the time dummy hedonic price index would be equal to the Jevons price index. See DeHaan (2010), equation (23), and Triplett (2006), p. 55.

(2003), and to the U.S. producer price indexes. Prior to 2004, my Jevons matched model (geometric mean) index and the PPI move quite closely, while my hedonic indexes showing a modestly higher rate of decline, as expected. The hedonic price indexes based on Intel list prices with and without TDP are virtually identical over the period beginning in 2000, through the beginning of 2005.

From 2004 through 2006, both my Jevons and hedonic price indexes decline much more slowly than the PPIs, while from 2006 through 2009 my Jevons and hedonic indexes fall at rates a little faster than the PPI. From 2009 to 2010 the Jevons and hedonic bracket the PPI. Finally, from 2010 through 2014, my hedonic indexes fall more slowly than the PPI, but all decline rates are in the low single digits. These are not the only hedonic price indexes for Intel processors available over this time span, and I discuss alternative estimates that others have constructed below.

Using almost the exact same hedonic regression model,[70] I also estimated a hedonic index using weekly data on retail internet pricing for desktop processor models that I had collected over the same time span. The data came from a now-defunct web site (sharkyextreme.com), which published the minimum weekly price quoted by a selection of national US internet retailers, over the period from the end of 2001 through the end of 2010. Similarly, I calculated a Jevons index based only on matched models in adjacent periods. These prices are a relatively limited subset of the much larger set of list prices for all Intel desktop processors, and presumably are more representative of lower end models most popular in the retail marketplace. Generally, the pattern over time is similar (steepest declines over 2001-2004 and 2006-2009, slower declines over 2004-2006 and 2009-2010).

[70] With one additional characteristic—a binary "OEM" indicator variable, indicating whether the product sold by the retailer came in a "boxed" retail package with heatsink and fan, or it came in "OEM" packaging without a fan, heat sink, and retail box. Monthly average prices were calculated from published weekly reports. The published weekly price was the reported minimum in a sample of larger internet component retailers.

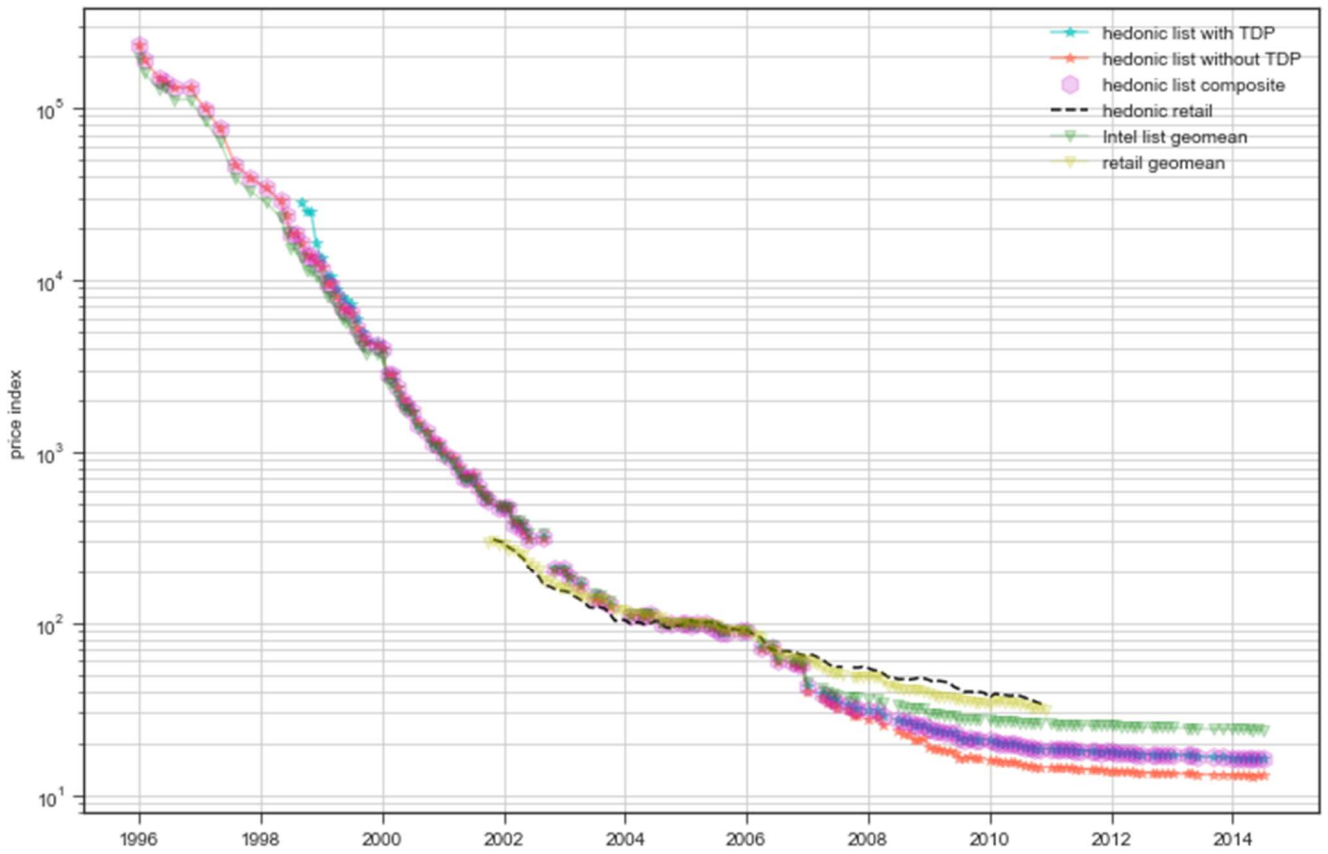


Figure 8. Matched model and hedonic price indexes for Intel desktop processors
January 2005=100

Table 7

Annualized compound rates of change in microprocessor price indexes

	Intel OEM List Prices			Intel Retail		BLS
	Hedonic w/TDP	Hedonic w/o TDP	Jevons Matched Model	Hedonic	Jevons Matched Model	Microproc PPI
1998m9-2001m12	-71.5%	-66.2%	-64.0%			-56.8%
2001m12-2004m4	-49.6%	-49.6%	-48.9%	-40.2%	-35.5%	-47.1%
2004m4-2006m1	-9.6%	-10.1%	-10.7%	-4.6%	-11.1%	-25.2%
2006m1-2009m1	-35.4%	-40.3%	-31.5%	-19.9%	-24.2%	-29.0%
2009m1-2010m11	-13.3%	-13.5%	-6.2%	-15.9%	-11.3%	-10.7%
2010m11-2014m7	-3.5%	-2.9%	-2.3%			-4.2%

Source: Author's dataset and calculations, except Microprocessor PPI, from BLS. See Appendix Table A.3.

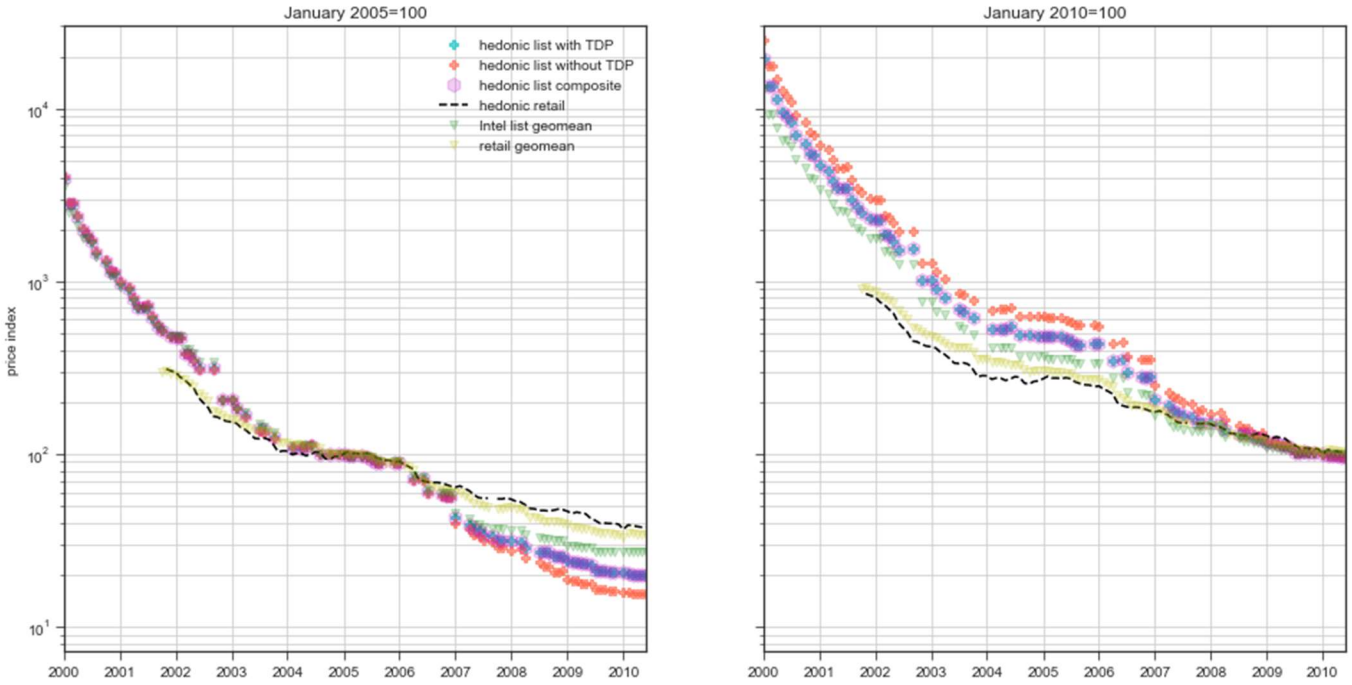


Figure 9 Jevons (Geometric Mean) and Hedonic Price Indexes with Alternative Base Periods

One interesting observation that emerges from these results is that, except for the period from 2006 through the end of 2007, all the Intel list price indexes, including both hedonic and geometric mean matched model (Jevons) indexes, move together in a fairly tight formation. This can be seen by comparing the original index (with January 2005=100) to rebased indexes with January 2010 = 100. (See Figure 9.) This is consistent with 2006-2007 being a highly atypical period, with many more older, exiting models (from now obsolete Pentium 4 branded architecture families), and new entering models (from its new Core 2 Duo branded architecture families) than has generally been the case for Intel historically, before or after this period. The change in Intel's product design strategies from 2006 through 2007, in responding to AMD's earlier technological challenge, has been commented upon by researchers,[71] and appears to have had impacts that are visible in these price indexes.

Although there are substantial differences in the magnitude of declines across different time periods and data sources, all the various price indexes I have constructed concur in showing

[71] "Note that in June 2006 there was intense competition for high performance chips with AMD selling the highest priced product at just over $1000. Seven chips sold at prices between $1000 and $600, and another five between $600 and $400. July 2006 saw the introduction of the Core 2 Duo and Fig. 2 shows that by October 2006; (i) AMD no longer markets any high performance chips (their highest price chip in October is just over two hundred dollars), and (ii) there are no chips offered between $1000 and $600 dollars and only two between $600 and $400 dollars. Shortly thereafter Intel replaces the non-Core 2 Duo chips with Core 2 Duo's.

Nosko goes on to explain how the returns from the research that went into the Core 2 Duo came primarily from the markups Intel was able to earn as a result of emptying out the space of middle priced chips and dominating the high priced end of the spectrum." From Pakes (2017), pp. 251-254, see also Nosko (2011) pp. 8-9.

substantially higher rates of decline in desktop microprocessor price prior to 2004, a stop-and-start pattern after 2004, and a dramatically lower rate of decline after 2010.

Taken at face value, this creates a puzzle. Even if the rate of innovation had slowed in particular for microprocessors, if the underlying innovation in semiconductor manufacturing technology had continued at the late 1990s pace (i.e., a new technology node every two years and roughly constant wafer processing costs in the long run), then manufacturing costs would continue to decline at a 30 percent annual rate, and the recent rates of decline in processor price just measured fall well short of that mark. Either the rate of innovation in semiconductor manufacturing must also have declined, or the declining manufacturing costs are no longer being passed along to consumers to the same extent, or both. The semiconductor industry and engineering consensus seems to be that the pace of innovation derived from continuing feature-size scaling in semiconductor manufacturing has slowed markedly. I next examine what other direct evidence is available.

Costs

Evidence on Manufacturing Costs. Microprocessors are a semiconductor product sold in truly large volumes. The overwhelmingly dominant player in this market, Intel, released a slide in a presentation to its stockholders in 2012 that supports the narrative of a slowing down in Moore's Law cost declines. (Table 8.) The figures from Intel's 2012 Investor Meeting seem to show accelerating cost declines in the late 1990s, rapid declines near a 30 percent annual rate around the millennium, followed by substantially slower declines in cost per transistor after the 45nm technology node (introduced at the end of 2007). As discussed previously, the transition to use of a larger wafer size after the 130nm technology node was accompanied by a particularly large reduction in transistor cost at the next node, using the larger size wafers.

		Transistor Cost Index, 90nm = 100		**Percent Transistor Cost Decline Rate**		**Compound Annual Decline Rate**	
		Otellini, 2012		Otellini, 2012		Otellini, 2012	
		Wafer Size		Wafer Size		Wafer Size	
Intro Date	Tech Node	200mm	300mm	200mm	300mm	200mm	300mm
1995q2	350	1575.35					
1997q3	250	1033.14		-34.4		-17.1	
1999q2	180	616.10		-40.4		-22.8	
2001q1	130	311.09		-49.5		-32.3	
2004q1	90		100.00		-67.9		-31.5
2006q1	65		48.87		-51.1		-30.1
2007q4	45		27.54		-43.6		-27.9
2010q1	32		17.69		-35.8		-17.9
2012q2	22		11.23		-36.5		-18.3
Intro dates: 130nm and up from http://www.intel.com/pressroom/kits/quickreffam.htm							
	< 130nm from ark.intel.com						

Table 8. Annualized decline rates for Intel transistor manufacturing cost, 2012
Source: Otellini (2012), digitized using WebPlotDigitizer.

Other Economic Evidence

Depreciation rates for semiconductor R&D. Another innovation metric in semiconductors is the depreciation rate for corporate investments in semiconductor R&D. As the rate of innovation increases (decreases), the stock of knowledge created by R&D should be depreciating more rapidly (less rapidly). One recent economic study estimates R&D depreciation rates in a number of high tech sectors, including semiconductors. The authors conclude that "the depreciation rate of the semiconductor industry shows a clear declining trend after 2000 in both datasets, albeit imprecisely measured."[72] This is consistent with a slowing rate of innovation.

Semiconductor fab lives. Faster (slower) technological change in semiconductor manufacturing should presumably shorten (lengthen) fab lifetimes. There are no recent studies of economic depreciation rates for semiconductor plant and equipment, but the anecdotal evidence on the 200mm fab capacity "reawakening" (detailed below) strongly suggests that fab lives have increased, consistent with a slowing rate of innovation in semiconductor manufacturing.

In August of 2018, Global Foundries (one of four remaining firms that had committed to development of leading edge logic manufacturing process technology) announced that it was abandoning its effort to move to its next targeted technology node (7nm), and would stick instead with its current generation technology. "'The lion's share of our customers…have no plans for' 7nm chips. Industry-wide demand for the 14/16 node was half the volume of 28nm, and 7nm demand may be half the level of the 14/16nm node, Caulfield said. 'When we look out to 2022, two-thirds of the foundry market will be in nodes at 12nm and above, so it's not like we are conceding a big part of this market,' he added."[73] This left only three remaining semiconductor manufacturing firms (Samsung, Intel, and TSMC) developing sub-10nm manufacturing technology, going forward into 2019.

A slowing pace of innovation in semiconductor manufacturing was even undeniable at Intel. Intel had introduced its 14nm technology node back in 2014 but ran into difficulties bringing its next generation 10nm technology to market. In August of 2018, Intel acknowledged that it was now delaying volume manufacturing of 10nm technology products until late 2019, over five years after its last technology node (i.e., almost triple its previous two-year 'tick-tock' cadence between new technology nodes), and almost three years after its initial projection (see Table 9 below).[74]

Personal computer replacement cycles. One reason for businesses and consumers replacing computers more frequently (less frequently) is if the rate of innovation in key components in computers, like microprocessors, increases (decreases), so performance improvements associated with replacement are more (less) economically compelling. While published studies of PC replacement cycles are scarce, Intel monitors replacement cycles for PCs, a major market for its desktop processors. In 2016, Intel CEO Brian Krzanich noted that PC replacement cycles had extended from four years, the previous average, to five or six years, the current average.[75] This, again, is consistent with a slower rate of innovation.

[72] Li and Hall (2015), p. 13.
[73] Merritt (2018); see also Moore (2018).
[74] Rogoway (2018), see also Cuttress and Shilov (2018).
[75] Krzanich (2016).

4. Is Moore's Law Still Alive? Intel's Perspective in Microprocessors

The most significant evidence against any current slowdown in semiconductor manufacturing cost reduction from Moore's Law had come from Intel. Fairly recent Intel statements about its manufacturing costs had been the primary factual evidence within the semiconductor manufacturing community countering the proposition that Moore's Law is ending. Unfortunately, Intel had not been consistent in the data it had presented publicly on this issue. Since late 2017, Intel appears to have refrained from releasing any new public information on its manufacturing costs.

The problem with Intel's previous statements is illustrated by Figure 10 and Table 9, which place side by side two exhibits on manufacturing costs per transistor that Intel has presented at its annual investor meetings—one in 2012 (by then-CEO Paul Otellini), and one in 2015 (by its top manufacturing executive, Bill Holt, see Figure 2). Some version of the right pane in Figure 10 had been the primary factual evidence in Intel assertions that Moore's Law continues at its historical pace. The graphics in Figure 10 have been digitized[76] and recorded in Table 9, then rebased to 100 at the 90nm technology node. Compound annual decline rates have been calculated in this table using quarterly introduction dates for the first processors manufactured by Intel at that technology node.

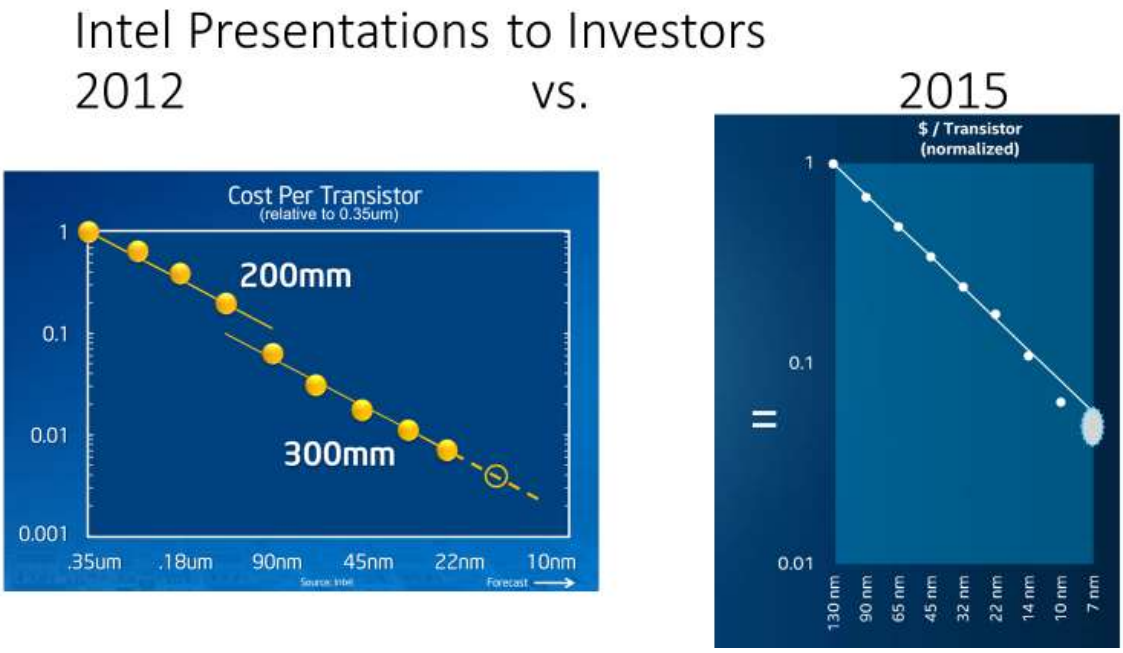


Figure 10 Intel Transistor Manufacturing Costs, 2012 vs. 2015 Versions
Source: Otellini (2012): Holt (2015).

[76] Using http://arohatgi.info/WebPlotDigitizer/.

The figures presented by Intel to shareholders in 2012 seem to show rapid declines in the 30 percent range around the millennium, then substantially slower declines in cost per transistor after the 45nm technology node (i.e., after 2007). In contrast, a more recent presentation by Intel in 2015 restates the more distant history to show very much slower declines in cost per transistor at earlier technology nodes. Intel has a stock disclaimer that numbers it presents are subject to revision, but in this case the revisions to the historical record are quite dramatic.

		Transistor Cost Index, 90nm = 100			**Percent Transistor Cost Decline Rate Between Nodes**			**Compound Annual Decline Rate**		
		Otellini, 2012		Holt, 2015	Otellini, 2012		Holt, 2015	Otellini, 2012		Holt, 2015
		Wafer Size			Wafer Size			Wafer Size		
Intro Date	Tech Node	200mm	300mm	300mm	200mm	300mm	300mm?	200mm	300mm	300mm?
1995q2	350	1575.35								
1997q3	250	1033.14			-34.4			-17.1		
1999q2	180	616.10			-40.4			-22.8		
2001q1	130	311.09		146.93	-49.5			-32.3		
2004q1	90		100.00	100.00		-67.9	-31.9		-31.5	-12.0
2006q1	65		48.87	71.26		-51.1	-28.7		-30.1	-15.6
2007q4	45		27.54	50.30		-43.6	-29.4		-27.9	-18.1
2010q1	32		17.69	35.64		-35.8	-29.1		-17.9	-14.2
2012q2	22		11.23	26.03		-36.5	-26.9		-18.3	-13.0
2014q3	14			16.13			-38.0			-19.2
2017q4?	10			9.46			-41.4			-21.1
Intro dates: 130nm and up from http://www.intel.com/pressroom/kits/quickreffam.htm										
	< 130nm from ark.intel.com									

Table 9. Comparison of Intel Cost per Transistor at Various Technology Nodes, 2015 vs. 2012

The 2015 graphic substantially revises what in the semiconductor industry would be considered the distant historical past (i.e., five technology nodes back from the 22nm node that was in production at the time the earlier 2012 presentation was given). Intel's most recent version of its history now shows transistors costs declining at 12-18% annual rates after the millennium, rather than the 30% annual declines it showed to its investors in 2012. Its transistor cost decline rate accelerates, rather than slowing further, at the most recent couple of technology nodes.

It now seems likely that one important reason for the restatement by Intel of its historical cost declines in 2015 was a definitional change in technical information made public by Intel. Instead of reporting transistor density (transistors per die area) based on actual die area and the number of transistors processed on an actual microprocessor die (which allows one to calculate an actual average transistors fabricated per die area), Intel apparently began using an entirely theoretical measure of area per designed transistor that appears not take into account the increasingly relaxed (from design rules) layout of transistors in actual die designs, imposed in part by the need to allow for additional area between transistors needed to fabricate increasingly complex interconnections.[77] (For die designs

[77] See Flamm (2017), p. 34, for a brief explanation of this issue. Intel's latest redefinition of its publicly disclosed "transistor density metric" is entirely theoretical: .6 x (transistors in a NAND logic cell/area of a NAND logic gate) + .4 x (transistors in a complex scan logic flip-flop cell/area of complex scan logic flip-flop cell) = # transistors/mm2.

released prior to 2010, Intel had previously disclosed both actual die size, and the number of transistors processed on the die, for many of its chip models.)

An Intel Exception?

Interpreting the recent economic history of Moore's Law, how can Intel's description of accelerating declines in manufacturing cost per transistor (as recently as September 2017[78]) be consistent with reports from other chip manufacturers, and their customers, of stagnating cost declines, or even cost increases? Increasingly important scale economies provide one plausible and coherent explanation.

Scale economies at the company level are obvious. The cost of a production scale semiconductor fab has increased dramatically at recent technology nodes, and only the very largest chip "IDMs" (Integrated Device Manufacturers) can depend on their internal demand to justify a fab investment. Intel made this case quite accurately at its 2012 Investor Meeting, predicting that only Samsung, TSMC, and itself would have the production volumes required to economically justify investment in leading edge fab technology for logic chips, by 2016.[79] (Intel overlooked GlobalFoundries, which by acquiring IBM's semiconductor business in 2015, substantially increased its scale.)[80] Both TSMC and GlobalFoundries are "pure" foundries, and achieve their volumes entirely by aggregating the demands of external chip design customers.

Many U.S.-based semiconductor companies have exited chip manufacturing (e.g. AMD, IBM) or stopped investing in leading edge fabrication while continuing to operate older fabs (Texas Instruments pioneered this so-called "fab-lite" strategy). Other "pure play" U.S. foundries (e.g., TowerJazz, On Semiconductor) operate mature foundry capacity that remains cost effective for lower volume chips. Long-established American chip companies, such as Motorola, National Semiconductor, and Freescale, disappeared in the course of mergers or acquisitions that continue to reshape the industry.

This consolidation in leading edge IC fabrication is global. In Europe, there are no manufacturers currently investing in leading edge technology.[81] In Asia, there are arguably only Toshiba in Japan, Samsung and Hynix in Korea, and foundry TSMC in Taiwan. Firm level scale economies explain why fewer firms can afford leading edge fabs, but can't explain why Intel's cost per transistor would have declined

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Such a definition does not allow for the practical effects of relaxation (from theoretical design rules) in actual cell layout needed, for example, to accommodate metal interconnections between logic cells. On Intel's new transistor density definition, see Mark Bohr, "Moore's Law Leadership," March 2017, available at https://newsroom.intel.com/newsroom/wp-content/uploads/sites/11/2017/03/Mark-Bohr-2017-Moores-Law.pdf.

[78] See Smith (2017), slide 6, "Is Moore's Law Dead? No!". Interestingly, since September of 2017, Intel has not—to the best of my knowledge—published a claim that its manufacturing cost per transistor continues to decline at rates exceeding previous historical decline rates, or is even falling at new technology nodes.

[79] Krzanich (2012), slide 19.

[80] What constitutes leading edge technology in memory chips is somewhat more nebulous, and several large memory specialist IDMs (Hynix, Toshiba, Micron) might also arguably be categorized as being near the leading edge. Global Foundries has since announced that it is dropping out of future development of new manufacturing technology nodes.

[81] The last remaining leading edge chipmaker headquartered in Europe, ST Microelectronics, announced in 2015 that it will be relying on foundries for future advance manufacturing needs.

much faster than at other producers still investing in leading edge fabs, particularly the foundries. It's possible that Intel has unique, proprietary technological advantages. A more mundane explanation is that product level scale economies drive these differences.

In particular, there has been an exponential increase in the costs of the ever more complex photomasks needed to pattern wafers using lithography tools—a set of masks cost $450,000 to $700,000 back in 2001, at 130nm, compared with a wafer production cost of $2,500 to $4,000 per wafer.[82] At 14nm, (updating wafer production costs using Intel costs in Table 9 implies 150% increases) wafer production cost would be $6,225 to $9,960. By contrast, costs for a mask set at 14nm are estimated to run from $10 million to $18 million, a 22- to 40-fold multiple of 130nm mask costs![27] Lithography cost models suggest that with 5000 wafers exposed per photomask set (a relatively high volume product at recent technology nodes), mask costs per unit of output will exceed both average equipment capital cost, and average depreciation cost. With smaller production runs for a product, photomask costs become the overwhelmingly dominant element of silicon wafer-processing cost at leading edge technology nodes.[83]

Intel, with the largest production runs in the industry (perhaps 300 to 400 million processors in 2014[84]), has huge volumes of wafers to amortize the cost of its masks, and is certainly benefitting from significant economies of scale. A single Intel processor design (and mask set) is the basis for scores of different processor models sold to computer makers. Processor features, on-board memory sizes, processor speeds, and numbers of functioning cores can be enabled or disabled in the final stages of chip manufacture, and manufacturing process parameters can even be altered to shift the mix of functioning parts in desired ways.[85]

For Intel, this creates average manufacturing costs per chip that are vastly smaller than costs for fabless competitors running much smaller product volumes using the same technology node at foundries. Foundries recoup those much higher per unit mask costs through one-time charges, or through high finished wafer prices charged to its fabless designer-customers. The customer directly bears the much higher design costs per unit if the latest technology node is chosen for the product.

Exponentially growing design and mask costs at leading edge nodes now make older technology nodes economically attractive for lower volume products. Higher variable wafer-processing costs per transistor at older nodes are more than offset by much lower fixed design and photomask costs.

Such scale-driven cost disadvantages are increasingly pushing low volume chip production to older chipmaking technology running in depreciated fabs. This is reshaping the economics of chip

[82] Both 130 nm mask and wafer cost estimates were presented by an engineer in Intel's in-house Mask Operation unit; Yang (2001). Mask set cost estimates at 14nm are taken from Black (2013), slide 6.

[83] Lattard (2014), slide 6.

[84] Based on the fact that Intel publicly revealed that it had shipped 100 million processors a quarter, a record-setting event, in the third quarter of 2014. Intel (2014), p. 1.

[85] When chips are tested after manufacture, the speed, power consumption, and functioning memory and feature characteristics are used to "bin" the processor into one of many different part numbers. As process yields improve over time with experience, new part numbers with faster speeds or lower power consumption, etc., are introduced. VanWagoner (2014) is a concise discussion by a former Intel manufacturing engineer of how a large variety of processor models are manufactured from a single unique processor design.

production, extending the economic lives of aging fabs. Older 200mm wafer fab capacity is now growing rapidly, forecast to expand almost 20% by 2020![86]

Historically, this is unprecedented. The additional 200mm capacity coming into service cannot use more advanced process technologies designed for 300mm wafer processing equipment. Much lower fixed design and photomask costs with older technology are the primary factor making it economically attractive for fabricating low volume products. As inexpensive computing penetrates into everyday appliances, "Internet of Things" chip designers are generating low volume foundry orders for chip designs tailored to market niches, filling these old fabs with chip orders that don't require the greatest possible density.

Is Intel an exceptional case in the semiconductor industry? Is its portrait of recently accelerating manufacturing cost declines reflected in the actual behavior of its product prices? The problem is, Intel does not disclose data on its product pricing to either the public, or government statistical agencies, so analysis of what an economist would call a quality-adjusted price is quite difficult.

Alternative Hedonic Price Indexes for Microprocessors. Apart from Intel's pre-2018 declarations of optimism, a second piece of evidence arguing against a slowdown in Moore's Law is a study by Byrne, Oliner, and Sichel (BOS, 2018), which also utilizes the same list price data from Intel (that I used) in making its argument. Using only the first four quarters of prices for recently introduced models, they run an annual time dummy hedonic price model over adjoining pairs of years, and find quality-adjusted prices declining at the same rate in 2000-04 as in 2009-13, at about a 42 percent annual rate of decline, and an even more impressive 46% decline over 2004-2009.[87] This is higher than any of the rates shown for 2004-2009, and very much higher than the decline rates post-2009 in Table 7.

The key differences between my hedonic price indexes and the BOS hedonic price indexes are: (1) BOS use only a subset of the desktop processors for which their chosen software benchmark scores are available (vs. all desktop processors listed on Intel's current price sheets); (2) BOS include quarterly average list prices for individual processors only during the first four quarters after their introduction onto the market (vs. using all available monthly average list prices); and (3) BOS use only a single processor characteristic (geometric mean of benchmark software performance scores[88]) in their hedonic model (vs. using a much larger set of processor characteristics that I argue is likely to be relevant to both demand and unit cost).

Sample Selection: SPEC benchmark vs no SPEC available. BOS acknowledge that there are some differences between chips which have benchmark (SPEC) scores available, and chips without (SPEC scores are primarily used to compare processor performance in servers and technical computing workstations, which generally use higher end processors than the consumer market).[89] They report that

[86] Dieseldorff (2016).

[87] Ibid. BOS (2018) use only the first four quarterly average prices for individual processors, and a single explanatory characteristic—performance on a software benchmark—in their hedonic regression.

[88] They take the geometric mean of processor performance on industry consortium SPEC's benchmark scores on single program integer and floating point software test suites. Their procedure for splicing the two or three distinct sets of benchmarks used over their sample period (SPEC2000 and SPEC2006, and possibly SPEC95) over their 2000-2013 sample period is not explicitly described. See Figure 4 above for evidence that both levels and slopes of these benchmarks change over time when they are compared.

[89] BOS (2018), Table 2.

a matched model price index using only the SPEC chips generally falls faster than an index using the non-SPEC chips in all time periods. They also report that their matched model indexes produce a qualitative pattern in price declines over time that is very similar to what is shown in Table 7, above, for all Intel desktop processors. Thus, these results suggest that the restriction of the price sample to higher performance processors with SPEC scores may bias estimates of quality-adjusted price declines toward higher rates of price decline, but is not responsible for the very different qualitative behavior over time (relatively constant, versus dramatic reductions in rates of decline after 2004).

First 4 quarters only, vs. all prices. BOS observe that individual Intel processor list prices very rarely change over time, on price sheets, after 2011, in contrast to the prior decade. They identify two scenarios they believe may explain this. In one scenario, "Intel offers progressively larger [but unobserved] discounts to selected purchasers as models age,"[90] producing a measurement error for older processors, but not recently introduced models. This would complicate estimation of hedonic price indexes using list price data. "The introduction period index would be unbiased even if there are unobserved discounts at the time of introduction provided that these discounts do not vary systematically over time or across models,"[91] while an index using all periods would presumably be biased.

Alternatively, they argue that even if the posted list prices are actual transactional prices, the older chips must be getting progressively more expensive in quality-adjusted terms if their nominal prices do not change, so relative demand for these models must be falling. "By focusing on prices [only] at the beginning of each model's life cycle, a regression that applies equal weights to all observations avoids over-weighting models whose quantities have dropped off."[92] These arguments are used to justify using only prices observed during the first four quarters after a model's introduction, discarding the majority of their sample of Intel list prices.

However, in a recent study, Sawyer and So (2017) replicate the substance of the BOS results over the period after 2009, in a sample utilizing only "early" (first 4 quarters after introduction) Intel list prices.[93] However, when processor characteristics are added to SPEC scores as explanatory covariates , Sawyer and So show that standard statistical tests decisively reject the exclusion of processor characteristics from a hedonic price equation which also includes SPEC scores.[94] When these other processor characteristics are not excluded, estimates of recent decline rates for quality-adjusted processor prices over time are dramatically smaller than those estimated by BOS.[95] We can reasonably conclude that it is the restriction of hedonic characteristics to benchmark scores only, and not the restriction to early prices, that is producing the pattern of unremittingly high price declines found in BOS(2018) over the post-2004 time period.

Sawyer and So also note that Intel processors are typically sold in their largest volumes only after the first four quarters in which they are available for sale.[96] Intel's own economic expert made this

[90] Byrne et. al. (2018), p. 690.
[91] Ibid.
[92] Ibid.
[93] Sawyer and So (2017), p. 8.
[94] Ibid., p. 11.
[95] Ibid., p. 10.
[96] Ibid., pp. 14-15.

point in its antitrust case before the European Commission, noting that processor production begins with a "ramp-up" phase that "begins with low volumes and typically lasts three to five quarters".[97] Therefore, using price data for a processor only during the first four quarters following its introduction likely would place relatively high weights on products actually being sold in relatively low volumes, compared to other products.

It seems reasonable to suggest that this may be a real world example of omitted variable bias, akin to that created in the last column of the perfect collinearity simulation in Table 6. However, BOS articulate some real concerns about use of Intel list price data to measure processor pricing trends. They note "a sharp change over the course of the 2000s in the life-cycle properties of Intel's posted prices…In the early period prices fell steeply over a model's life cycle. However, by 2011-2012, price paths are flat or nearly so, with only a few instances of sizable price declines."[98] These observations are spot on.

Figure 11 shows the fraction of incumbent (i.e., omitting newly introduced products) desktop processor prices that changed from one list price sheet to the next one issued, from 1998 through mid-2014. Through mid-2014, it is evident that Intel's propensity to alter list prices on existing processors diminished over time, though it never entirely stopped adjusting list prices on its existing product line through mid-2014. In 2008 and 2009, for example, there were price sheets on which anywhere from 35 to 40 percent of already introduced desktop processor prices changed from the previous sheet.[99] Since 2014, however, existing processor prices rarely if ever change from one price sheet to the next.

Indeed, if one had to choose a date based on this chart for a climacteric in Intel pricing practices, 2010—the year after its antitrust cases were settled—would seem a promising choice. That year also apparently coincides with the beginning of a determined campaign by Intel to raise its profit margins, an effort that seems to have had some success (aided at that point by a greatly diminished competitive threat from its historical rival, AMD). (See Figure 12.) Raising its average sales prices (ASP) was a key element of this strategy. (See Figure 13.)

In earlier versions of their research, BOS focused on the evident change in Intel pricing strategies during the first decade of the 2000's as the motivation for restricting their Intel prices to "early" initial processor prices.[100] Their hypothesis, that Intel may have changed its pricing strategy during the first decade of the new millennium, actually seems quite plausible, given that the European Commission launched a major antitrust case against Intel over it processor price discounting practices during the 2002-2006 period, culminating in a preliminary decision against Intel in 2007, and a final decision in 2009.[101] A related private U.S. antitrust case by Intel's rival, AMD, was filed, then settled in 2009.

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[97] European Commission (2009), p. 326.

[98] BOS (2018), p. 687.

[99] BOS (2018), Figure 4, show a similar set of patterns over time in the share of Intel desktop processors with a list price decline within 4 quarters of introduction.

[100] In the earlier 2017 Federal Reserve working paper version of their study, BOS speculated that "[i]t is possible that Intel actually changed its life-cycle pricing strategy to extract more revenue from older models, with the posted prices reflecting this change." Byrne, Oliner, and Sichel (2017), p. 8.

[101] See European Commission (2009). The same antitrust concerns also resulted in government antitrust actions in Japan and Korea, and by the U.S. Federal Trade Commission. Acting on an appeal by Intel, the European Court of Justice sent the EU case back to a lower court for further consideration in 2017, so this seems destined to be litigated for years to come.

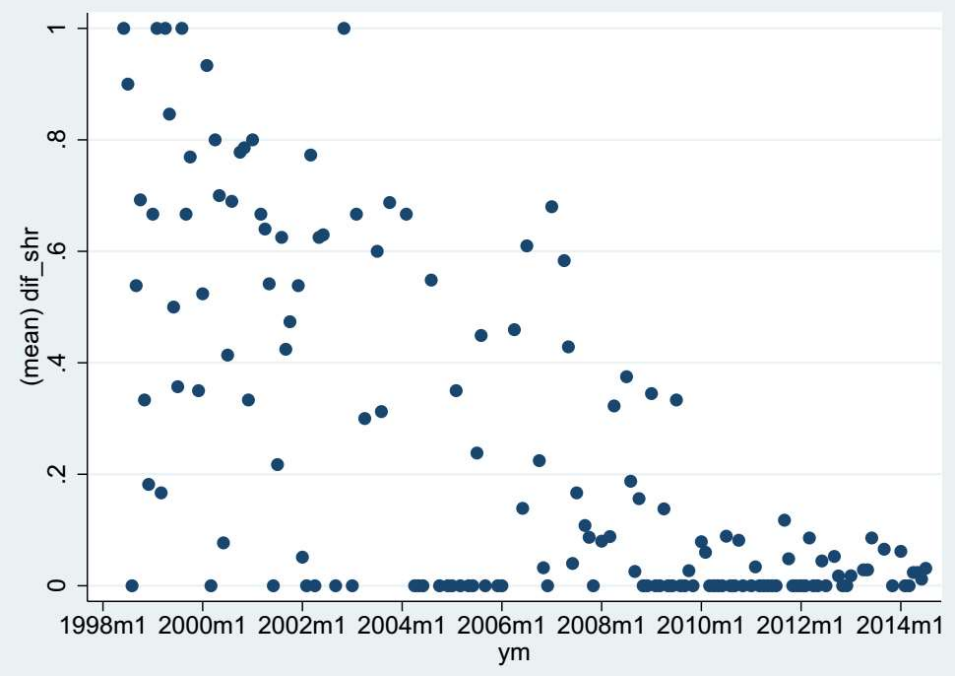

Figure 11. Fraction of Intel desktop processor prices changing from one price list to the next.
Source: Author's tabulation from Intel list price dataset.

Figure 12. Intel's post-2010 gross margin elevation objective
Source: Smith (2015).

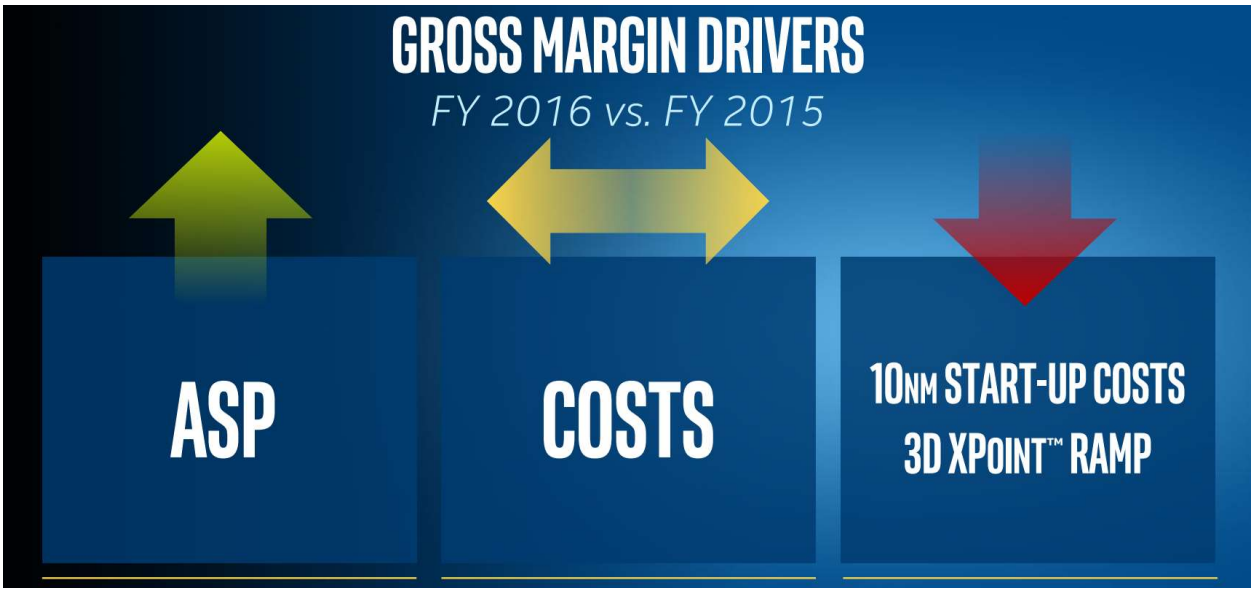

Figure 13. Intel's 2015 explanation to its shareholders for success in maintaining high profit margins
Smith (2015).

The BOS (2018) scenario of "progressively larger discounts to selected purchasers as models age" is difficult to test, since no data on Intel transaction prices for its wholesale sales to large buyers are publicly available. We do know that evidence produced in the EU antitrust investigation seems to show that even the newest chips sold to large OEM customers were heavily discounted from list prices prior to 2006, at times with conditional exclusivity rebates that were not publicly reported by Intel or its customers.[102]

However, there is one public source of Intel transactional price data that is real, observed, and does not require any assumptions about unobserved behavior. Retail prices in the electronics industry are linked to wholesale prices, directly and indirectly. Most directly, the very largest retailers can purchase boxed processors directly from Intel, or like smaller retailers, from distributors. (Approximately 20% of Intel processors in recent years, by volume, were sold directly as boxed processors, primarily to small computer makers and electronic retailers.[103]) Computer original equipment manufacturers

[102] See European Commission (2009). See also *SEC v. Dell Inc. et al. Complaint* (2010), which asserts that unreported exclusivity rebates given by Intel to Dell had climbed to about ¾ of Dell's operating income by 2006.
[103] "Although it sells microprocessors directly to the largest computer manufacturers, such as Dell, Hewlett Packard, and Lenovo, its Channel Supply Demand Operations (CSDO) organization is responsible for satisfying the branded boxed CPU demands of Intel's vast customer network of distributors, resellers, dealers, and local integrators. Intel's boxed processor shipment volume represents approximately 20 percent of its total CPU shipments…Processors ship from CW1 to one of four CW2 "boxing" sites, which kit the processors with cooling solutions (e.g., fan, heat sink) and place them in retail boxes and distribution containers. Such boxing sites are typically subcontracted companies that ship the boxed products to nearby Intel CW3 finished-goods warehouses where they are used to fulfill customer orders. Channel customers range in size and need; they are mostly low-volume computer manufacturers and electronics retailers." B.Wieland, P. Mastrantonio, S. P. Willems, and K. G. Kempf, "Optimizing Inventory Levels Within Intel's Channel Supply Demand Operations," *Interfaces*, Vol. 42, No. 6, Nov–Dec 2012, pp. 517–18.

(OEMs), electronics system manufacturers, and electronic parts distributors who purchase processors directly from Intel can resell excess inventories to other distributors, resellers, and retailers, and these actually show up on the retail market labeled as "OEM package" (vs. "Retail Box" packaging).

Both boxed and OEM-packaged processors are sold by retailers, distributors, and brokers, with a price that is advertised publicly and directly observable in the marketplace. (The retail data used in constructing my matched model price index include both OEM and retail packaged chips sold by internet retailers.) The retail data used in Table 7 also seem to clearly point to a deceleration in microprocessor price declines after 2004.

It seems reasonable to presume that retail transaction prices (which are observable in the market), at least in the long run should have some stable stochastic relationship to wholesale producer transactional prices. Indeed, a least one previous study found such linkages between OEM contract transactional prices and retail prices for high volume chips sold in the semiconductor industry.[104]

There are market-driven economic reasons behind this linkage. Both semiconductor manufacturers and their OEM customers sell their excess inventories of chips to brokers and distributors during industry downturns, pushing small buyer spot prices down in distributor and retail sales channels as excess OEM inventories of chips are absorbed in those sales channels. In tight markets, conversely, when semiconductor manufacturers are capacity constrained, wholesale contract prices to large OEMs rise. To meet surging demand, OEMs may even try to purchase additional volumes of chips, beyond the volumes negotiated in contracts with chip manufacturers, in retail and distribution markets. As both large OEMs and smaller buyers compete fiercely over the remaining, unallocated output, upward pressure on retail and distributor prices is felt. In short, both direct and indirect linkages between small buyer (retail and distributor) markets, and large buyer (contracts with OEMs) markets, as well as arbitrage across distribution channels would lead an economist to expect to observe a structural relationship between observed retail processor prices, and unobserved large OEM wholesale prices.

In a still earlier version of their research, BOS (2015) had speculated that the change in Intel pricing behavior (resulting in a systematic change in the relationship between Intel list prices and unobserved OEM contract prices) may have occurred after 2006.[105] This is actually an interesting and plausible choice of dates for a change in Intel pricing behavior, since it coincides approximately with the end of the exclusivity rebates that had been the subject of the government and private antitrust actions mentioned earlier. There is also a significant drop in the maximum fraction of Intel list prices changing between adjacent price sheets evident after 2006 visible in Figure 11 (the last occasions on which 60% of prices for existing processors were changed were at the end of 2006 and early 2007). If there was a structural shift in Intel pricing practices that caused list price to diverge more sharply from actual transactional prices after 2006, we might then also expect to see a change in the relationship between movements in observed transactional prices in the retail market, and Intel list prices after 2006. This is testable using observational data.

[104] See Flamm (1993), for a study documenting linkages between retail prices and OEM contract prices for DRAM memory chips.

[105] "By 2006, this pattern had completely changed; the posted price of a specific model tended to remain constant, even after a new, higher performance model became available at a similar price." BOS (2016), p. 9.

I explored the possibility that there was some detectable change in the relationship between Intel list (posted wholesale) prices and observed retail prices after 2006 by constructing a panel of monthly observations on average retail price and posted list price covering 163 distinct Intel desktop processor models sold by Internet retailers over the years 2000 through 2010.[106] I allow for model fixed effects (which permits a particular low-end Celeron model, for example, to be related to Intel list price with a different retail margin than a high end Core i7 model). The model that I estimated specified the log of retail price as

$$\ln(R_{it}) = a_i + b \ln(I_{it}) + c\, Age_{it} + d\, OEM + After2006 + e\, After2006 \times \ln(I_{it}) + f\, After2006 \times Age_{it} + u_{it},$$

with R_{it} an observation on average retail price for model i in month t; I_{it} the average posted Intel list price in a month in which list price had been posted at least once; Age_{it} the number of elapsed months since the month the model's price had been first posted on a published Intel price sheet; After2006 a binary indicator variable with value 1 in 2006 and thereafter, zero before; OEM a binary indicator for whether the product sold was the retail boxed version, or the bare chip in OEM packaging; and u_{it} a random disturbance term. If post-2006 transaction prices reflect age discounts from Intel list price that pre-2006 prices did not, we would expect to find a statistically significant shift coefficient on the interaction of After2006 with Age.

Table 10 shows the results of estimating this model.[107] The After2006 shift variable, and all of its interactions, including interactions with processor model Age, are close to zero and statistically insignificant individually, and jointly.[108] The relatively flatter trajectories over time for Intel list prices after 2006 are mirrored in the behavior of flatter retail price trajectories for the same chips.

Therefore, based on the only evidence on actual transaction prices that is publicly available, i.e., advertised retail prices from Internet-based vendors, there is no evidence of some structural change occurring after 2006 in the relationship between observed Intel list price and observed retail market prices. Of course, this does not directly prove that there was no change in the relationship between Intel list prices and (unobserved) discounted OEM contract prices for processors, but it certainly weighs against it.

Figure 11 and our earlier discussion suggests that 2010-11 is another candidate time period in which to search for shift in Intel pricing practices. Unfortunately, the retail data analyzed in Table 10 does not extend past this date.

[106] This is the same sharkyextreme.com data I previously used to construct Jevons and hedonic retail price indexes.
[107] Robust standard errors clustered on processor model are shown in Figure 8.
[108] The Wald F(3,162) test statistic for the joint hypothesis that all After2006 terms were zero was .82, the p-value .49.

Table 10

Fixed Effects Model of Log Retail Price For Intel Desktop Processors

	(Full Model)	(Constrained Model)
	lp_ret	lp_ret
lp_tray [log Intel Tray Price]	0.763***	0.768***
	(15.37)	(17.93)
oem	-0.0497***	-0.0496***
	(-6.70)	(-6.77)
age	-0.00676***	-0.00582***
	(-3.70)	(-4.91)
1.aft2006	0.0204	
	(0.13)	
1.aft2006#age	0.00162	
	(0.83)	
1.aft2006#lp_tray	-0.0108	
	(-0.39)	
_cons	1.347***	1.303***
	(4.87)	(5.55)
N	1580	1580
R-sq	0.987	0.987
adj. R-sq	0.986	0.986

t statistics in parentheses
* p<0.05, ** p<0.01, *** p<0.001

SPEC scores vs. chip characteristics. As previously remarked, Sawyer and So (2017) have shown that the BOS results showing no slowdown in quality-adjusted Intel processor price declines since 2000 are not the result of using only "early" Intel list prices, but instead are driven primarily by use of SPEC benchmark scores as the sole characteristic in a hedonic model, in lieu of a more extensive set of chip characteristics.

The use of SPEC scores instead of actual chip characteristics is based on the argument that direct performance measures are easier to get right than relevant chip characteristics. But this argument overlooks three fundamental reasons why chip characteristics should still be included in a hedonic price equation.

First, there is a computer architecture literature that tells us that benchmark scores of a CPU on any given task should be well explained by a small set of chip characteristics, including numbers of cores and threads, computer architectural design, chip clock rate, and on-chip memory cache sizes. This literature actually identifies the chip characteristics that are relevant, and even uses them to model computer CPU performance out of sample.[109] As I next show, scores on various SPEC processor

[109] Hennessey and Patterson(2003), in the Third Edition of their classic computer architecture textbook, pp. 59-60, do exactly this to compare the Pentium III with a Pentium 4 operating at the same clock rate.

benchmarks are almost perfectly predicted by a linear function of the small set of chip characteristics that the computer design literature predicts are its determinants.

Second, economics tells us that the characteristics that belong in a hedonic price equation are there because they are relevant to user demand, but that they have an additional effect on price if they alter supplier marginal cost.[110] At best, software benchmark scores might correctly serve as a perfect summary measure of quality perceived by users, on the demand side. But there is no reason, technological or economic, why a measure of chip performance relevant to demand should also perfectly capture the separate effects of underlying characteristics that determine performance, on chip cost. Omitting variation in processor characteristics that affects chip cost will induce omitted variable bias in the hedonic coefficient estimates, if the omitted characteristics' effects on cost are correlated (but not perfectly collinear) with the included benchmark scores.

That is, assume for the sake of argument that the mix of user demands for various types of computer applications was fixed over time, and that processor performance on this fixed weight mix of computer applications was correctly captured in some SPEC benchmark. Even with the heroic assumption that this aggregated benchmark correctly captured everything relevant to chip quality on the demand side (and it is clear it does not[111]), there is no plausible technological or economic reason why variations across chip models in marginal production costs related to chip characteristics that determine benchmark scores, should be perfectly mirrored by variation in SPEC benchmark scores.

Indeed, the computer architecture literature teaches us that a variety of chip characteristics can affect performance, and that, therefore, the same SPEC score can potentially be produced with diverse, non-unique combinations of numbers of cores, threads, cache memory, clock frequency, etc. In fact, if we look at actual SPEC scores, multiple distinct chip models can produce approximately the same score. But variation in each of these chips' characteristics—cores, threads, on-chip memory, and clock frequencies—may have very different impacts on production cost for the processor compared with impact on SPEC scores.

Third, if benchmark scores are determined by chip characteristics, using chip characteristics directly in the hedonic equation—instead of, or in addition to a single benchmark score —effectively allows coefficients in the hedonic equation to change to mirror changes in the average mix of tasks run by computer users over time. Use of a single benchmark or fixed-weight index of benchmarks effectively assumes the mix of tasks relevant to performance for users is fixed over time.[112]

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[110] Pakes (2003), p. 1581, equation 3, notes that the hedonic price function can be interpreted as the sum of the expected marginal cost, conditional on characteristics, and expected markup (derived from the demand function), conditional on characteristics. The key point is that the product characteristics are arguments in the separate cost and demand function terms in the hedonic price equation.

[111] Since power draw minimization, graphics, and hardware virtualization capabilities clearly are desirable to large subsets of computer users, yet will have no direct impact on SPEC scores if missing or disabled in a processor.

[112] That is, assume we have two benchmarks, b1 and b2, and two processor characteristics, c1 and c2. Assume b1 = a1 c1 + a2 c2, while b2 = e1 c1 + e2 c2. Assume users in the aggregate run b1 applications 50% of the time, b2 applications the other 50%. Then we can represent performance on the "average market workload" with a performance index that looks like .5 b1 + .5 b2, or equivalently, .5 (a1 c1 + a2 c2) + .5 (e1 c1 + e2 c2) = [.5 (a1+e1)] c1 + [.5 (a2 + e2)] c2. That is, the benchmark index is equal to a simple linear function of the two characteristics. Now, if the weights of b1 and b2 change to 25% and 75% on the new "market workload," workload performance will be incorrectly captured by the original performance index (50% weights) even if scaled by some arbitrary

For all these reasons, use of the SPEC score as the sole characteristic in a hedonic price equation is not a highly plausible economic assumption. In addition, because SPEC scores are only available for the subset of Intel desktop processors used by OEMs in servers, the use of SPEC scores in a desktop processor hedonic price regression will considerably reduce sample size compared with statistical models using chip characteristics but not SPEC scores. In the Intel list price data, the number of Intel desktop processors with SPEC scores available for analysis is a fraction of all Intel desktop processors with list prices available in any time period. When using other publicly available retail or distributor desktop processor price data, an even larger fraction of the available data may not have SPEC scores available. [113]

To support this point, I next demonstrate that SPEC processor benchmark scores are almost perfectly predicted by a small number of underlying chip characteristics, and provide little or no additional information. In making this claim, I note that I make use of a set of processor microarchitecture dummy variables in the set of chip characteristics used. Neither Sawyer and So, nor BOS, use processor architecture dummy variables (which I have shown make an important contribution to the explanatory power of a hedonic price model) in the set of characteristics they employ when estimating a chip characteristic-based hedonic model. It is quite possible that adding a software benchmark score to a set of chip characteristics that excludes the architectural dummies has the effect of capturing much of the effect of these dummy variables in the hedonic price model.

The role of different chip characteristics on different SPEC benchmarks, however, varies greatly across different types of SPEC benchmarks, which argues for direct use of the underlying characteristics in a hedonic equation. It is an argument for letting the data decide what the correct weights on processor characteristics in a hedonic price equation are, rather than adopting the implicit weights embedded within a time invariant weighted average benchmark score.

5. Chip Characteristics and Computer Performance: Building Blocks for A Hedonic Analysis

By forcing us to focus on the relationship between performance of microprocessors on representative software benchmarks—which all agree should be an important determinant of chip demand-- and chip characteristics, BOS have a done us a great service in providing focus for a discussion of what chip characteristics should be used when estimating a hedonic price equation for microprocessors.

The theoretical computer architecture literature makes use of a *processor performance equation* to predict processor performance. Effectively, this relationship models the execution time a computer processing unit takes to perform some given software benchmark program (i.e., a given sequence of programming instructions) as the product of two parameters: average clock ticks per instruction and the seconds per clock tick in the processor's clock.[114] Since a processor performance benchmark score is

constant. However, performance on "market workload" is still correctly captured by a linear function of the two underlying chip characteristics (though the coefficients of the characteristics in this function change). The specification that is linear in the underlying characteristics is simply more flexible in representing shifts in demand.

[113] Because the selection of processors commonly sold to consumers for use in desktop PCs may include relatively fewer desktop processors used in servers (the ones which would have SPEC scores available).

[114] See Hennessey and Patterson (2012), section 1.9, pp. 48-52.

proportional to the inverse of time required to run a benchmark program on a particular computer processor, we can invert the processor performance equation and then have

Performance ~ IPC x clock rate ,

where **IPC** is processed **instructions per clock** tick, clock rate is measured in ticks per second, and the performance index basically compares benchmark instructions executed per unit time across processors. Indeed, given a particular computer architecture, computer engineers simply scale measured performance linearly by clock rate in order to model the approximate impact of raising clock rate on processor performance.[115]

IPC will depend on both the design (architecture) of the computer processor and the particular mix of instructions being executed in the benchmark software. The specified clock rate of a processor model is typically fixed after testing, at the end of the chip fabrication process.[116] "Binning" during testing of finished chips creates different speed grade bins, which are subsequently sold as different processor models to computer manufacturers and other consumers. The effective, yielded mix of non-defective, more valuable fast processors, and less valuable slow processors, on a fabricated wafer containing hundreds or thousands of these processors, is a determinant of processor manufacturing costs.

Speed is not the only chip processor characteristic that is affected by random fabrication process variation. There may also be random manufacturing variation affecting the voltage needed to run the chip properly, varying from die to die on the same wafer. Chips which require less power to perform correctly may be identified through testing, and sold as low power models of the processor.[117]

Microprocessor chips generally have on-chip caches of fast local memory which can also affect the execution time for given software. The portion of on-chip cache memory which is defect-free, and therefore usable by the chip, can also vary with the incidence of manufacturing defects during the fabrication process, and testing then leads to additional binning of finished chips by usable, functional cache memory.

Similarly, particular sections of chip circuitry associated with some advanced features of the chip may not be fully functional due to random processing defects. In order to maximize revenue from all usable products yielded from a finished silicon wafer, a complex system of testing "bins" based on speed, memory, power requirements, and working feature functionality is used to define distinct processor models sold as different chips to final consumers. Indeed, chips are generally designed with some redundant circuitry and electrical "fusing" options intended to maximize saleable product, and

[115] Hennessey and Patterson(2003), in the Third Edition of their classic computer architecture textbook, pp. 59-60, do exactly this to compare Pentium III performance with a Pentium 4 operating at the same clock rate.
[116] Random variation in a highly complex semiconductor manufacturing process leads to a distribution of functional chips by the maximum clock rate at which they can successfully execute some test suite. A "fast" processor can operate at a higher than average clock frequency, while a "slow" processor can only operate correctly at a slower than average clock rate.
[117] And processing of the wafer can be optimized to produce relatively more chips requiring less power.

revenues, from a processed wafer with dies that may not be perfect. A dozen processor models may be derived from a single, artfully designed die manufactured in the thousands on a single wafer.[118]

At Intel, microprocessor designs are identified with a "microarchitecture," which historically is associated with a publicly available codename. (For example, the processor microarchitecture launched by Intel in October 2017 was given the codename "Coffee Lake".[119]) Prior to 2010, Intel also made public information on its processors' die sizes and the number of transistors on the die processed in its manufacture. Based on this information (which is no longer publicly released), it appears the many dozens of microprocessor models for each of its microarchitectures were based on somewhere between one and three basic die designs.[120] That is, the dozens of different processor models corresponding to a single microarchitecture product family were manufactured from just one to three basic chip designs fabricated on silicon wafers.

It is straightforward to analyze the relationship between SPEC scores and microprocessor characteristics. Table 10 shows the results from estimating a linear regression model explaining log SPEC scores with a set of explanatory variables suggested by the computer engineering literature: a full set of microarchitecture dummy variables (since IPC is going to depend on computer microarchitecture), log of the base processor clock rate, a dummy variable indicating a "turbo" feature is enabled on the chip (the highest clock rate achievable by a single core on the chip will differ from the base processor clock rate if this feature is available), log of on-chip memory cache size,[121] log of number of physical processor cores on the chip, and a dummy variable indicating that multithreaded "virtual" logical cores are available on a chip.[122] In addition, a binary indicator variable for use of "autoparallelization" in compiling the SPEC benchmark software code is included, since that can enable a speedup on multicore processors, or on processors with multithreading.[123]

A simple log linear regression model that explains SPEC benchmark performance as a function of six processor characteristics (and a full set of 29 to 31 dummy variables for different Intel x86 processor

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[118] The design of a chip will segment the circuitry into functional blocks which can be disabled electronically (e.g., with programmable "fuses") during the manufacture and testing process. Some redundant circuitry is typically made part of the design, to maximize yield of usable parts after test. A more capable chip can generally be made less capable by disabling portions of its circuitry at the final stages of manufacture. This may done deliberately by manufacturers to create additional supplies of lower end chips when customer demand for lower end parts exceeds the portion of output physically binned into low end chip models on the basis of test results.

[119] https://gizmodo.com/intels-latest-coffee-lake-processors-are-fast-as-hell-1819129322 .

[120] Prior to 2010, Intel publicly released the exact die area and number of "processing transistors" used in manufacturing most of its microprocessor models. All processors with exactly the same microarchitecture, die area, and numbers of processing transistors can be assumed to be derived from a single die design. Analysis of this data shows anywhere from 1 to 3 unique microarchitecture/die size/processing transistor combinations were being used to produce many dozens of processor models.

[121] Actually, I am using the size of the "last level cache," since microprocessors can have a hierarchy of successively larger (and slower) caches onboard.

[122] Hyperthreading is Intel's name for multithreading capability, additional circuitry added to the processor which creates two logical (or "virtual") processors that can access every physical core. One logical processor can begin processing the next instruction while the other logical processor is actually executing an instruction in a core, thus allowing a form of chip-level parallelism which can speed up performance when a computer program spawns multiple threads.

[123] Indeed, after a short number of months at the beginning of the SPEC 2006 suite in 2006, almost all the single process SPEC benchmark scores have autoparallelization turned on.

microarchitectures) accounts for a remarkable 97 to 98 percent of the variation in SPEC2006 benchmark scores for thousands of computer models using Intel x86 processors over the 2005-2017 period. (Table 11.) Note that this regression utilizes all Intel x86 desktop, server, and mobile processors in the SPEC2006 database, and further, that it is estimated using every different individual computer making use of an included processor as the underlying set of observations used in estimating the model.

Table 11 Log of SPEC 2006 benchmark as function of processor characteristics
Six Characteristics Model

Dependent variable is log of

	SPECf06	SPECi06	SPECfr06	SPECir06
lproc	0.196***	0.115**	0.383***	0.429***
	(0.0401)	(0.0396)	(0.0590)	(0.0746)
lcache	0.0965**	0.0861***	0.140**	0.109***
	(0.0283)	(0.0232)	(0.0442)	(0.0208)
lcores	0.157***	0.0385	0.642***	0.826***
	(0.0284)	(0.0285)	(0.0357)	(0.0249)
ht	0.0644**	0.0318**	0.132***	0.201***
	(0.0179)	(0.0111)	(0.0169)	(0.0130)
lmaxmhz	0.514***	0.722***	0.101	0.328***
	(0.0651)	(0.0560)	(0.103)	(0.0747)
autop	0.0649*	0.00310	0.0107	-0.0134
	(0.0262)	(0.0534)	(0.0211)	(0.0362)
Microarchitecture dummies	Y	Y	Y	Y
Observations	1160	1190	2207	2417
R-squared	0.966	0.960	0.982	0.974
N_clust	31	31	29	30
r2_within	0.687	0.697	0.896	0.893

Cluster robust standard errors in parentheses, clustered on Intel microarchitecture.
* p<0.05, ** p<0.01, *** p<0.001

lproc: log base processor clock rate
lmaxmhz: log of maximum clock rate if turbo mode available
lcores: log of number of physical cores in processor
ht: binary dummy variable for hyperthreading
lcache: log of amount of last level cache memory on processor chip
autop: autoparallelization enabled in compiler when SPEC software was compiled, dummy variable

That is, variation in chipsets, motherboards, configured memory, and other components in the computer systems from different manufacturers making use of any particular chip model, which is reflected in the residual, accounted for no more than 2 to 4 percent of observed variation in SPEC scores. This analysis utilizes individual tested computer system data; i.e., on average there are 4 to 5 different computer systems using a specific processor model.

We can alternatively calculate a median or mean score across all computer systems utilizing each processor chip model, to more closely resemble the BOS procedure for deriving a single SPEC score for each chip model. Using that as the basis for our SPEC2006 performance regression model, we get an even higher R^2, of about .99.[124] (Table 12.) It is clear that computer architecture dummies and five processor characteristics, together, essentially perfectly predict SPEC benchmark scores.

[124] I drop all chips shown as underclocked or overclocked by computer system maker (having reported clock rate more than 10Mz slower or faster than the Intel-specified base clock rate), and ignore autoparallelization in calculating medians or means in Table 12. Table 12 reports results using logs of medians; using logs of means would give almost identical results.

Table 12 Log of median SPEC 2006 benchmark as function of processor characteristics
Five Characteristics Model

Dependent variable is log of median computer system score for particular processor model

	SPECf06	SPECi06	SPECfr06	SPECir06
lproc	0.279***	0.156***	0.507***	0.460***
	(0.0347)	(0.0338)	(0.0767)	(0.0565)
lcache	0.0783**	0.0575**	0.155**	0.122***
	(0.0259)	(0.0194)	(0.0531)	(0.0184)
lcores	0.190***	0.0697*	0.644***	0.810***
	(0.0254)	(0.0274)	(0.0513)	(0.0167)
ht	0.0721***	0.0371***	0.134***	0.211***
	(0.0133)	(0.00727)	(0.0132)	(0.00788)
lmaxmhz	0.421***	0.677***	-0.0109	0.286***
	(0.0716)	(0.0526)	(0.105)	(0.0575)
Microarchitecture dummies	Y	Y	Y	Y
Observations	331	340	449	454
R-squared	0.988	0.985	0.990	0.994
N_clust	30	30	28	28
r2_within	0.843	0.853	0.941	0.975

Cluster robust standard errors in parentheses, clustered on Intel microarchitecture.
* p<0.05, ** p<0.01, *** p<0.001

Two points are significant. First, the coefficients of (weights assigned to) different processor characteristics in determining SPEC scores are very different for different SPEC benchmarks. The clear implication is that different processor characteristics can have very different effects on performance for different types of workloads. A flexible hedonic price model, reflecting a changing distribution of chip consumers across distinct types of workloads, would best let the empirical data decide the weights users place on particular characteristics, rather than aggregating the characteristics into a single benchmark score with the time-invariant weights implicitly used to perform the aggregation into a performance metric.

Second, these characteristics also will affect cost. Every distinct Intel microarchitecture is manufactured using a single fabrication technology node, so in addition to representing the processor's design architecture, the microarchitecture dummies also capture variation in microprocessor manufacturing cost that is induced by variation in chip microarchitectures and manufacturing technology. As previously described, different quality grades (measured by processor clock rates, amounts of on-chip cache memory, and chip features) produced by testing and binning are also associated with cost differences. Coefficients on these characteristics in a hedonic reduced form price equation should be regarded as reflecting both demand and cost effects.

Finally, in addition to the chip characteristics determining SPEC performance, there are a small set of additional chip characteristics that we would certainly want to include in a hedonic price equation for microprocessors. Power dissipated by a chip determines whether expensive cooling solutions are required, shifting demand for that processor; power requirements are also important (for battery life) in mobile applications. Electricity use, the principle variable cost of computing, will vary with power consumed. Further, power dissipation varies with random manufacturing process variations, so the power rating of a chip is also going to be related to chip cost. Whether or not a graphics processor is integrated into the microprocessor will also affect both demand and cost for that chip. Support for

hardware virtualization will have no practical effect on processor performance on SPEC benchmarks, but is a valuable feature for business customers wishing to increase server efficiency by running numerous "virtual machines" on their servers simultaneously.

In conclusion, we should remember that SPEC scores are maintained by organizations that sell servers, processors used in servers, and the largest server customers, so a SPEC-selected sample will be skewed toward the models of chips that perform best as server processors. The SPEC performance regressions in Tables 11 and 12 would then seem to tell us that desktop and server performance should be modelled separately, with different weights placed on different chip characteristics.

This suggests a natural segmentation of microprocessors for purposes of price measurement. a desktop segment oriented toward single software program application performance, a mobile (laptop and tablet) segment tilted toward both performance and low power, and a server segment with a greater emphasis on performance on embarrassingly parallel workloads (servers running a mix of uncoordinated applications with performance more like the SPEC "rate" benchmarks). In terms of finding public data useful in estimating a hedonic price equation, retail/distribution prices will be most readily observable and useful in estimating desktop microprocessor prices. Retail data will be much more limited and less useful for mobile processors, and even more limited and therefore least useful, for hedonic measurement of server processor prices.

The absence of a reliable source of producer transactional data for microprocessors, for use in government price indexes, is a serious and increasingly formidable barrier to measuring prices and innovation correctly in the semiconductor industry.

6. Conclusion

There is considerable evidence that semiconductor manufacturing innovation has historically been responsible for perhaps a 20-30% annual decline in the cost of manufacturing transistors on a chip. One would expect that this predictable cost decline would be transformed into a similar price decline in a competitive industry, at least in the long run, and therefore, that a decline of this magnitude would serve as a floor on the long-run trajectory of semiconductor prices for high volume semiconductor products. Innovations in the architecture and designs being manufactured on the chip, new kinds of chip designs, and superior performance characteristics of existing designs fabricated using more advanced fabrication technology, would be additional factors explaining even higher long run rates of decline in quality-adjusted semiconductor prices.

Historically, most high-volume semiconductor applications ultimately migrated to more advanced manufacturing technology nodes, pulled there by the simple economics of continuing declines in cost using more advanced fabrication technology. This pressure now seems to have lessened, in part the result of rapidly increasing fixed costs sunk into the design of new chips using the most advanced manufacturing technology, and, in part due to an apparent slackening in the rate of cost decline at the technological frontier of semiconductor manufacturing.

The available empirical evidence, on balance, suggests that Moore's Law-related historical declines in chip manufacturing cost have clearly been attenuated over the last decade. For chips where market price data are collected, decline rates in chip prices over time seem to have greatly diminished. The evidence for exceptionality in Intel microprocessor price declines is shaky, indicative primarily of

poor quality public data, speculations about Intel pricing behavior, and likely, of omitted variables in hedonic price models.

A substantial economic literature has connected faster innovation in semiconductor manufacturing to rapidly improving price-performance for semiconductors, to larger price declines for information technology, to increased uptake of IT across the economy, and higher rates of labor productivity growth. If correct, this implies that a slowdown in semiconductor manufacturing innovation, and attenuation of price declines in both chips and IT, may play an important role in current stagnation in labor productivity growth.

Finally, it is now almost an article of faith in high tech industry that an expanding cloud of computing and machine intelligence is in the process of transforming our economy and society. Much of this faith is built on projection into the future based on past experience with increasingly powerful and pervasive computing capability that both cost less and used less energy, year after year. The winding down of Moore's Law means that the technological scaling that drove these historical declines, and implicitly underlie the most optimistic assumptions about the spread of ubiquitous computing in the future, may no longer hold. Both cost and energy use now seem more likely to increase in lockstep with the scale of cloud computing in the future. Unless there are continuing, significant improvements in software technology, computing costs—and energy use—are unlikely to decline, or even stay constant as computing capacity increases, as was true in the past. Investments in entirely new technologies will be needed, as will a renaissance of creativity and innovation in software, the neglected sibling living in the shadow cast by Moore's Law—dramatically cheapening hardware—for the last 50 years.

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Appendix Table A1.

SPEC CPU Benchmark	Coef. CAGR	Robust Std. Err.	z	P>|z|	[95% Conf.	Interval]	N	R2	# CPUs
1995m5-2000m3									
int95	.5826577	.0175146	33.27	0.000	.5483296	.6169857	152	.92	41
fp95	.6397016	.0231907	27.58	0.000	.5942486	.6851546	142	.90	41
int95_rate	.6241582	.0273672	22.81	0.000	.5705194	.677797	54	.87	20
fp95_rate	.7227752	.0331	21.84	0.000	.6579003	.7876501	47	.83	18
2000m11-2004m11									
int2000	.3304092	.0173773	19.01	0.000	.2963503	.3644681	215	.80	76
fp2000	.3429411	.023522	14.58	0.000	.2968389	.3890433	203	.81	73
int2000_rate	.4697731	.0512966	9.16	0.000	.3692337	.5703125	160	.77	59
fp2000_rate	.3989549	.0351676	11.34	0.000	.3300276	.4678822	162	.84	59
2005m2-2007m1									
int2000	.3222474	.016442	19.60	0.000	.2900217	.3544732			
fp2000	.3365855	.022279	15.11	0.000	.2929195	.3802515			
int2000_rate	.4650892	.0475414	9.78	0.000	.3719098	.5582686			
fp2000_rate	.3986346	.032545	12.25	0.000	.3348476	.4624217			
2005m6-2012m11									
int2006	.1709304	.0069587	24.56	0.000	.1572916	.1845691	689	.84	254
fp2006	.2467286	.0077563	31.81	0.000	.2315266	.2619306	690	.87	254
int2006_rate	.2472256	.013015	19.00	0.000	.2217167	.272734	728	.62	278
fp2006_rate	.2537211	.0101781	24.93	0.000	.2337725	.2736698	711	.76	261
2013m1-2016m5									
int2006	.1687175	.0064265	26.25	0.000	.1561218	.1813133			
fp2006	.2414989	.0070952	34.04	0.000	.2275926	.2554053			
int2006_rate	.2417978	.0119286	20.27	0.000	.2184181	.2651774			
fp2006_rate	.2480768	.0093352	26.57	0.000	.2297801	.2663735			

Notes:
intxx and fpxx are SPEC CPU integer and floating point base scores (no special compiler optimizations used) when single instance of benchmark run on CPU.

intxx_rate and fpxx_rate are SPEC CPU scores with multiple instances of benchmark programs run simultaneously; number of instances is entirely at discretion of entity running benchmark—may be as high as maximum number of threads, but may also be maximum number of cores, or any number less than that (on processors with symmetric multithreading capability—Intel version is branded as "hyperthreading"—additional program execution hardware in a CPU core allows as many as two threads to simultaneously share a single core's remaining hardware).

Model estimated was
ln(SPEC CPU benchmark) = a + b * monthly date of initial CPU availability in any manufacturer's computer hardware + c * autoparallelization indicator + d * time shift indicator x monthly date of initial CPU availability in tested hardware.

where
autoparallelization = 1 if autoparallelization turned on at compile time for 2006 benchmark, 0 otherwise
time shift indicator = 1 if year > 2004 for SPEC 2000 benchmarks, 0 otherwise
= 1 if year > 2012 for SPEC 2006 benchmarks, 0 otherwise
Annualized growth rate estimated as exp(b + d* timeshift indicator)^12 -1

Time shift indicators were statistically significant, as were autoparallelization indicators.

Appendix Table A2

Stata Simulation Code for Simulated Hedonic Model With Perfect Collinearity

```
clear all
set obs 10000000
set seed 3492673
gen  arch_dum =  round(runiform())
gen  time =round(runiform())
gen  clock_rate = 1000+500*round(runiform()) +500*time
gen  turbo =  round(runiform())
tab arch_dum time
tab clock_rate time
tab turbo time

gen  speed = clock_rate + 500*arch_dum + 200*turbo
gen  mfg_cost = 50 +  2* clock_rate + 2000* turbo + 500*arch_dum -10 * time
gen  p= 100 + 2 *speed + mfg_cost + 1000*runiform()
* = 600 + 2 *speed + mfg_cost + mean zero uniform disturbance
* = 650 + 4* clock_rate + 1500 archdum + 22* turbo -10 * time //drop speed

corr time turbo arch_dum clock_rate speed
regress p speed time clock_rate arch_dum
estimates store drop_turbo
regress p speed time arch_dum turbo
estimates store drop_clock
regress p speed time clock_rate turbo
estimates store drop_arch
regress p time clock_rate arch_dum turbo
estimates store drop_speed
* with misspecification
regress p speed time
estimates store speed_only
regress p speed time turbo
estimates store speed_turbo
regress p speed time arch_dum
estimates store speed_arch
regress p speed time clock_rate
estimates store speed_clock
esttab drop_speed drop_turbo drop_clock drop_arch  speed_only , se r2 star
```

Appendix Table A.3 Chained Price Indexes

Date	Jevons Matched Model Intel List	Hedonic Intel List w/TDP	Hedonic Intel List w/o TDP	Composite Hedonic Intel List	Jevons Matched Model Retail	Hedonic Retail
January-96	196383.56		232447.02	231447.62		
February-96	159569.90		191462.78	190639.58		
May-96	129798.20		150059.80	149414.61		
June-96	132226.40		143241.33	142625.47		
August-96	112359.33		131195.84	130631.77		
November-96	112359.33		131486.64	130921.31		
February-97	84382.60		99329.64	98902.57		
May-97	64371.61		76736.96	76407.03		
August-97	39060.86		46984.07	46782.06		
November-97	32751.36		39463.75	39294.07		
February-98	28491.35		34435.32	34287.27		
May-98	23179.48		28976.31	28851.73		
June-98	18954.30		23740.89	23638.82		
July-98	15152.91		18823.58	18742.65		
August-98	15152.91		18830.84	18749.88		
September-98	13352.15	28349.97	16362.79	16292.44		
October-98	11403.35	24872.67	13991.48	13931.32		
November-98	11331.73	24872.67	13761.40	13702.23		
December-98	10514.36	16480.79	12793.36	12738.35		
January-99	9878.41	13411.71	11784.04	11733.37		
February-99	8111.81	10616.32	9459.32	9418.65		
March-99	8088.11	10555.94	9433.53	9392.97		
April-99	6943.28	8955.80	8040.34	8005.77		
May-99	5964.09	8006.00	6988.77	6958.72		
June-99	5694.12	7696.46	6682.05	6653.32		
July-99	5411.72	7295.62	6361.84	6334.49		
August-99	4582.74	5928.07	5268.22	5245.57		
September-99	4076.54	4954.04	4694.43	4674.25		
October-99	3749.09	4418.23	4322.18	4303.59		
December-99	3693.52	4260.07	4219.85	4201.70		
January-00	3552.64	3998.98	4016.25	3998.98		
February-00	2518.33	2798.82	2840.01	2798.82		
March-00	2518.33	2807.36	2849.88	2807.36		
April-00	2120.15	2355.55	2400.74	2355.55		
May-00	1775.42	1982.94	2031.68	1982.94		
June-00	1759.27	1847.23	1882.56	1847.23		
July-00	1627.95	1710.10	1742.91	1710.10		
August-00	1382.75	1460.25	1486.94	1460.25		
October-00	1235.76	1301.81	1327.46	1301.81		
November-00	1079.50	1137.71	1160.14	1137.71		
December-00	1051.38	1108.52	1130.41	1108.52		
January-01	918.65	969.08	987.77	969.08		
March-01	866.15	906.17	923.62	906.17		
April-01	766.52	793.57	808.82	793.57		
May-01	687.62	710.82	724.23	710.82		
June-01	687.62	709.58	722.75	709.58		
July-01	678.95	721.34	734.86	721.34		
August-01	595.44	616.80	625.27	616.80		
September-01	549.37	553.45	559.49	553.45		
October-01	524.04	519.80	522.31	519.80	297.08	
November-01					304.24	310.65
December-01	482.80	479.26	481.76	479.26	291.62	303.23
January-02	478.88	470.72	472.45	470.72	286.75	297.98
February-02	478.88	470.95	472.81	470.95	270.88	278.13
March-02	401.62	384.38	384.60	384.38	268.82	269.14
April-02	401.62	379.62	379.83	379.62	254.87	252.82
May-02	381.46	349.44	346.87	349.44	247.15	239.21
June-02	339.33	314.99	311.33	314.99	222.93	211.45
July-02					213.61	197.87
August-02					201.82	185.72
September-02	339.33	317.17	310.47	317.17	178.12	165.45
October-02					174.96	163.73
November-02	204.88	208.53	206.03	208.53	167.25	158.28
December-02					161.35	154.59
January-03	204.88	208.63	206.16	208.63	158.85	153.42
February-03	182.28	185.78	183.61	185.78	156.96	150.71
March-03					149.93	143.22
April-03	172.62	167.50	164.64	167.50	145.13	138.08
May-03					140.15	131.24
June-03					136.78	123.30
July-03	148.35	141.66	136.97	141.66	137.66	122.50
August-03	144.53	138.15	133.61	138.15	137.03	123.68
September-03					136.13	121.44
October-03	133.83	126.95	123.19	126.95	128.82	113.45
November-03					117.26	102.81
December-03					117.41	104.27
January-04					117.39	104.00
February-04	112.91	108.68	108.94	108.68	112.79	99.37
March-04					113.34	100.94
April-04	112.91	108.89	110.06	108.89	113.26	100.56
May-04	112.91	109.02	110.26	109.02	109.86	97.81
June-04	112.91	112.39	113.36	112.39	108.52	99.62
July-04					109.25	102.80
August-04	100.00	100.44	99.93	100.44	107.86	102.06
September-04					101.70	94.38
October-04	100.00	100.37	100.52	100.37	99.24	93.23
November-04					99.70	96.37
December-04	100.00	99.95	99.94	99.95	99.59	97.14
January-05	100.00	100.00	100.00	100.00	100.00	100.00
February-05	96.84	98.27	98.42	98.27	100.40	103.38
March-05	96.84	98.30	98.46	98.30	99.31	100.94
April-05					99.15	100.96
May-05	96.84	98.54	98.68	98.54	99.00	100.26
June-05	96.84	95.26	95.46	95.26	97.40	101.43
July-05	95.66	92.93	93.62	92.93	96.01	99.96
August-05	90.92	88.38	89.05	88.38	91.72	95.69
September-05	90.92	88.42	89.11	88.42	90.16	93.78
October-05					89.56	92.30

Date	Jevons Matched Model Intel List	Hedonic Intel List w/TDP	Hedonic Intel List w/o TDP	Composite Hedonic Intel List	Jevons Matched Model Retail	Hedonic Retail
November-05					89.20	91.89
December-05	90.92	89.80	89.21	89.80	89.72	89.96
January-06	90.92	89.52	88.78	89.52	89.98	90.81
February-06					86.42	86.93
March-06					83.70	84.67
April-06	75.21	71.79	70.46	71.79	81.47	81.55
May-06					72.00	72.80
June-06	74.09	72.58	71.32	72.58	69.19	70.00
July-06	62.14	60.99	59.36	60.99	66.88	68.78
August-06					64.06	68.22
September-06					63.26	68.48
October-06	60.06	58.53	57.14	58.53	62.21	68.03
November-06	59.74	57.36	56.22	57.36	62.36	66.54
December-06	59.74	57.46	56.36	57.46	61.08	65.09
January-07	45.37	42.79	39.79	42.79	60.04	64.27
February-07					59.27	65.26
March-07					57.38	63.25
April-07	42.07	39.24	36.59	39.24	54.96	61.28
May-07	39.31	36.72	34.25	36.72	52.40	58.14
June-07	39.13	36.12	33.70	36.12	51.30	55.86
July-07	37.57	34.29	31.81	34.29	50.52	55.51
August-07					49.20	55.51
September-07	37.09	33.60	31.17	33.60		
October-07	36.58	31.48	28.66	31.48	48.63	55.04
November-07	36.58	31.50	28.72	31.50	48.39	54.96
December-07					48.80	55.63
January-08	36.39	31.41	27.45	31.41	48.74	54.64
February-08					48.55	53.17
March-08	36.13	30.95	27.94	30.95	48.11	52.71
April-08	34.16	28.70	25.22	28.70	45.97	50.78
May-08					43.16	48.37
June-08					42.79	48.10
July-08	33.15	27.18	23.56	27.18	42.01	47.09
August-08	32.24	26.95	22.40	26.95	40.91	47.14
September-08	32.19	26.92	22.42	26.92	40.51	46.80
October-08	31.56	25.68	20.81	25.68	40.80	47.24
November-08	31.56	25.60	20.66	25.60	40.41	47.95
December-08	31.56	25.41	21.14	25.41	40.06	47.62
January-09	29.23	24.19	18.92	24.19	39.24	46.60
February-09	29.23	23.82	18.58	23.82	37.49	45.23
March-09	29.23	23.86	18.61	23.86	37.36	46.09
April-09	28.59	23.11	17.95	23.11	37.17	45.58
May-09	28.59	23.10	17.95	23.10	37.01	44.99
June-09	28.59	22.84	17.73	22.84	36.21	42.45
July-09	27.33	21.18	16.39	21.18	35.68	41.25
August-09	27.33	21.11	16.35	21.11	34.70	39.74
September-09	27.33	21.25	16.50	21.25	34.80	39.82
October-09	27.27	20.90	16.22	20.90	34.59	39.61
November-09	27.27	20.91	16.23	20.91	34.15	39.64
December-09					34.06	39.18
January-10	27.10	20.61	16.00	20.61	33.10	36.67
February-10	26.97	20.39	15.82	20.39	34.83	38.81
March-10	26.97	20.09	15.59	20.09	34.85	38.46
April-10	26.97	20.11	15.61	20.11	34.18	38.11
May-10	26.97	19.96	15.51	19.96	34.13	37.70
June-10	26.97	19.97	15.52	19.97	33.96	37.84
July-10	26.35	19.27	14.99	19.27	33.77	37.65
August-10	26.35	19.03	14.82	19.03	33.08	36.75
September-10	26.35	18.92	14.74	18.92	32.10	35.69
October-10	25.98	18.66	14.54	18.66	31.75	34.91
November-10	25.98	18.62	14.51	18.62	31.51	33.93
December-10					31.24	33.65
January-11	25.98	18.63	14.52	18.63		
February-11	25.51	18.43	14.37	18.43		
March-11	25.51	18.45	14.39	18.45		
April-11	25.51	18.46	14.39	18.46		
May-11	25.51	18.51	14.39	18.51		
June-11	25.51	18.19	14.19	18.19		
July-11	25.51	18.20	14.20	18.20		
September-11	25.37	17.99	14.07	17.99		
October-11	25.18	17.87	13.98	17.87		
November-11	25.18	17.70	13.87	17.70		
December-11	25.18	17.79	13.83	17.79		
January-12	25.18	17.83	13.83	17.83		
February-12	25.18	17.60	13.66	17.60		
March-12	24.98	17.47	13.55	17.47		
April-12	24.98	17.47	13.56	17.47		
May-12	24.98	17.48	13.56	17.48		
June-12	24.79	17.32	13.52	17.32		
July-12	24.79	17.32	13.52	17.32		
September-12	24.61	17.28	13.50	17.28		
October-12	24.56	17.06	13.37	17.06		
November-12	24.56	17.14	13.44	17.14		
December-12	24.56	17.15	13.44	17.15		
January-13	24.53	16.94	13.25	16.94		
April-13	24.48	16.92	13.24	16.92		
May-13	24.50	16.94	13.26	16.94		
June-13	24.26	16.73	13.19	16.73		
September-13	24.13	16.57	13.14	16.57		
November-13	24.13	16.53	13.12	16.53		
January-14	24.01	16.42	13.03	16.42		
February-14	24.01	16.42	13.03	16.42		
March-14	24.01	16.43	13.04	16.43		
April-14	23.96	16.18	12.92	16.18		
May-14	23.91	16.17	12.86	16.17		
June-14	23.93	16.18	12.87	16.18		
July-14	23.85	16.36	13.05	16.36		

Appendix Table A.4 Regression Summary Statistics, Estimated Time Dummy Coefficients, and Price Relatives
Intel List Price Hedonic Model without TDP

month ending	time dummy	std error	degs of free dom	t-statistic	p value	num obs	number arch fixed effects	r2 total	r2 within	bias-corrected price relative	percent change from prev observation	month ending	time dummy	std error	degs of free dom	t-statistic	p value	num obs	number arch fixed effects	r2 total	r2 within	bias-corrected price relative	percent change from prev observation
1996m2	-0.195	0.04	2	-4.43	0.05	5	1	0.99	0.99	0.82	-17.63	2006m1	-0.006	0.04	78	-0.14	0.89	90	4	0.95	0.94	1.00	-0.48
1996m5	-0.249	0.09	4	-2.68	0.06	7	1	0.91	0.91	0.78	-21.62	2006m4	-0.232	0.04	77	-5.31	0.00	89	4	0.95	0.93	0.79	-20.64
1996m6	-0.061	0.17	2	-0.37	0.75	5	1	0.94	0.94	0.95	-4.54	2006m6	0.011	0.04	68	0.30	0.76	80	4	0.97	0.96	1.01	1.21
1996m8	-0.099	0.14	2	-0.70	0.56	5	1	0.97	0.97	0.92	-8.41	2006m7	-0.185	0.05	78	-3.39	0.00	91	5	0.93	0.91	0.83	-16.77
1996m11	0.000	0.07	5	0.00	1.00	8	1	0.95	0.95	1.00	0.22	2006m10	-0.040	0.06	88	-0.70	0.48	101	5	0.92	0.88	0.96	-3.73
1997m2	-0.286	0.09	6	-3.04	0.02	10	2	0.93	0.93	0.76	-24.46	2006m11	-0.019	0.07	69	-0.26	0.79	82	5	0.91	0.89	0.98	-1.62
1997m5	-0.271	0.14	8	-1.94	0.09	13	3	0.95	0.83	0.77	-22.75	2006m12	0.000	0.07	52	0.00	1.00	64	6	0.92	0.89	1.00	0.25
1997m8	-0.500	0.10	11	-4.78	0.00	16	3	0.96	0.78	0.61	-38.77	2007m1	-0.353	0.08	48	-4.19	0.00	61	6	0.91	0.83	0.71	-29.40
1997m11	-0.176	0.05	11	-3.25	0.01	16	3	0.99	0.75	0.84	-16.01	2007m4	-0.085	0.05	45	-1.76	0.09	57	6	0.97	0.87	0.92	-8.03
1998m2	-0.139	0.07	13	-1.91	0.08	20	4	0.98	0.57	0.87	-12.74	2007m5	-0.068	0.05	45	-1.28	0.21	56	6	0.97	0.83	0.94	-6.41
1998m5	-0.176	0.08	13	-2.21	0.05	20	4	0.98	0.64	0.84	-15.85	2007m6	-0.018	0.06	46	-0.30	0.76	57	5	0.96	0.88	0.98	-1.60
1998m6	-0.200	0.03	13	-7.48	0.00	19	3	0.99	0.96	0.82	-18.07	2007m7	-0.060	0.06	55	-0.96	0.34	67	5	0.95	0.86	0.94	-5.61
1998m7	-0.233	0.03	16	-6.79	0.00	22	3	0.99	0.92	0.79	-20.71	2007m9	-0.022	0.06	63	-0.36	0.72	75	5	0.93	0.84	0.98	-2.00
1998m8	0.000	0.03	19	0.00	1.00	26	4	0.99	0.92	1.00	0.04	2007m10	-0.087	0.07	50	-1.19	0.24	61	4	0.93	0.85	0.92	-8.05
1998m9	-0.141	0.04	20	-3.61	0.00	27	4	0.98	0.89	0.87	-13.11	2007m11	0.000	0.06	39	0.00	1.00	48	3	0.95	0.89	1.00	0.19
1998m10	-0.158	0.05	19	-3.47	0.00	26	4	0.97	0.91	0.86	-14.49	2008m1	-0.048	0.07	48	-0.69	0.50	59	5	0.93	0.84	0.96	-4.42
1998m11	-0.018	0.04	18	-0.40	0.69	25	4	0.98	0.92	0.98	-1.64	2008m3	0.016	0.07	61	0.23	0.82	72	5	0.92	0.78	1.02	1.81
1998m12	-0.075	0.06	16	-1.25	0.23	22	3	0.97	0.89	0.93	-7.03	2008m4	-0.105	0.07	61	-1.45	0.15	71	4	0.92	0.77	0.90	-9.74
1999m1	-0.084	0.05	17	-1.65	0.12	24	4	0.98	0.94	0.92	-7.89	2008m7	-0.071	0.07	56	-1.02	0.31	66	4	0.93	0.79	0.93	-6.59
1999m2	-0.221	0.04	18	-6.28	0.00	25	4	0.99	0.97	0.80	-19.73	2008m8	-0.053	0.07	61	-0.77	0.45	71	4	0.93	0.78	0.95	-4.92
1999m3	-0.003	0.02	19	-0.15	0.88	24	3	1.00	0.99	1.00	-0.27	2008m9	-0.001	0.07	68	-0.02	0.98	78	4	0.92	0.77	1.00	0.07
1999m4	-0.160	0.03	20	-5.70	0.00	25	3	0.99	0.97	0.85	-14.77	2008m10	-0.077	0.07	62	-1.10	0.28	72	4	0.92	0.77	0.93	-7.17
1999m5	-0.141	0.05	22	-3.03	0.01	27	3	0.97	0.90	0.87	-13.08	2008m11	-0.009	0.07	60	-0.14	0.89	72	5	0.93	0.79	0.99	-0.72
1999m6	-0.046	0.05	23	-0.88	0.39	28	3	0.96	0.84	0.96	-4.39	2008m12	0.021	0.07	58	0.32	0.75	70	5	0.94	0.79	1.02	2.35
1999m7	-0.051	0.06	23	-0.88	0.39	28	3	0.95	0.78	0.95	-4.79	2009m1	-0.114	0.07	53	-1.71	0.09	65	5	0.94	0.75	0.89	-10.53
1999m8	-0.191	0.07	21	-2.84	0.01	26	3	0.95	0.78	0.83	-17.19	2009m2	-0.020	0.06	53	-0.33	0.74	65	5	0.94	0.76	0.98	-1.80
1999m9	-0.117	0.06	19	-2.11	0.05	25	3	0.96	0.87	0.89	-10.89	2009m3	0.000	0.06	49	0.00	1.00	60	4	0.95	0.80	1.00	0.17
1999m10	-0.084	0.05	26	-1.85	0.08	33	4	0.98	0.89	0.92	-7.93	2009m4	-0.038	0.06	50	-0.66	0.51	61	4	0.95	0.81	0.96	-3.56
1999m12	-0.024	0.03	35	-0.82	0.42	42	4	0.99	0.92	0.98	-2.37	2009m5	-0.001	0.05	52	-0.02	0.98	63	4	0.95	0.82	1.00	0.02
2000m1	-0.050	0.03	38	-1.58	0.12	45	4	0.98	0.92	0.95	-4.82	2009m6	-0.014	0.05	57	-0.27	0.79	68	4	0.96	0.82	0.99	-1.24
2000m2	-0.348	0.04	31	-8.95	0.00	38	4	0.98	0.93	0.71	-29.29	2009m7	-0.079	0.04	58	-1.89	0.06	69	4	0.97	0.84	0.92	-7.51
2000m3	0.003	0.03	38	0.12	0.91	45	3	0.99	0.97	1.00	0.35	2009m8	-0.003	0.03	56	-0.12	0.90	67	4	0.99	0.92	1.00	-0.27
2000m4	-0.172	0.03	53	-5.39	0.00	60	3	0.97	0.95	0.84	-15.76	2009m9	0.009	0.03	60	0.32	0.75	73	5	0.98	0.92	1.01	0.90
2000m5	-0.168	0.05	55	-3.63	0.00	62	3	0.94	0.90	0.85	-15.37	2009m10	-0.017	0.03	64	-0.59	0.56	77	5	0.98	0.91	0.98	-1.68
2000m6	-0.078	0.05	54	-1.59	0.12	61	3	0.94	0.90	0.93	-7.34	2009m11	0.000	0.03	63	0.00	1.00	76	5	0.98	0.90	1.00	0.05
2000m7	-0.078	0.03	51	-2.57	0.01	58	3	0.97	0.96	0.93	-7.42	2010m1	-0.015	0.04	74	-0.40	0.69	88	6	0.96	0.84	0.99	-1.41
2000m8	-0.160	0.04	52	-4.31	0.00	59	3	0.96	0.94	0.85	-14.69	2010m2	-0.012	0.03	87	-0.35	0.73	101	6	0.96	0.83	0.99	-1.11
2000m10	-0.114	0.03	52	-3.76	0.00	59	3	0.97	0.96	0.89	-10.73	2010m3	-0.015	0.04	80	-0.42	0.68	94	6	0.96	0.84	0.99	-1.46
2000m11	-0.135	0.03	51	-4.76	0.00	58	3	0.97	0.95	0.87	-12.60	2010m4	0.001	0.04	73	0.02	0.98	87	7	0.96	0.86	1.00	0.15
2000m12	-0.026	0.03	53	-0.91	0.37	60	3	0.97	0.94	0.97	-2.56	2010m5	-0.007	0.04	78	-0.20	0.84	91	6	0.95	0.85	0.99	-0.67
2001m1	-0.135	0.03	56	-4.52	0.00	63	3	0.96	0.93	0.87	-12.62	2010m6	0.000	0.04	83	0.00	1.00	96	6	0.95	0.84	1.00	0.06
2001m3	-0.067	0.02	54	-2.89	0.01	60	2	0.97	0.95	0.94	-6.49	2010m7	-0.035	0.04	83	-0.97	0.34	96	6	0.95	0.83	0.97	-3.40
2001m4	-0.133	0.03	48	-4.34	0.00	54	2	0.95	0.92	0.88	-12.43	2010m8	-0.012	0.04	87	-0.34	0.74	100	6	0.95	0.82	0.99	-1.13
2001m5	-0.111	0.03	44	-3.88	0.00	50	2	0.96	0.93	0.90	-10.46	2010m9	-0.006	0.03	88	-0.18	0.86	101	6	0.95	0.82	0.99	-0.57
2001m6	-0.002	0.02	41	-0.10	0.92	47	2	0.97	0.96	1.00	-0.20	2010m10	-0.014	0.03	85	-0.41	0.68	98	6	0.95	0.83	0.99	-1.35
2001m7	0.016	0.03	44	0.49	0.63	50	2	0.95	0.92	1.02	1.68	2010m11	-0.002	0.03	86	-0.07	0.94	99	6	0.95	0.83	1.00	-0.19
2001m8	-0.162	0.04	53	-4.06	0.00	60	3	0.95	0.91	0.85	-14.91	2011m1	0.000	0.03	96	0.00	1.00	111	7	0.95	0.83	1.00	0.06
2001m9	-0.112	0.04	64	-2.85	0.01	71	3	0.93	0.88	0.89	-10.52	2011m2	-0.011	0.03	109	-0.34	0.73	125	7	0.94	0.81	0.99	-1.01
2001m10	-0.070	0.05	70	-1.50	0.14	77	3	0.88	0.82	0.93	-6.64	2011m3	0.000	0.03	111	0.01	0.99	127	7	0.94	0.81	1.00	0.09
2001m12	-0.082	0.05	71	-1.78	0.08	78	3	0.86	0.78	0.92	-7.76	2011m4	0.000	0.03	110	0.00	1.00	126	7	0.94	0.80	1.00	0.05
2002m1	-0.020	0.04	74	-0.49	0.63	82	4	0.89	0.77	0.98	-1.93	2011m5	-0.001	0.03	117	-0.02	0.98	133	7	0.94	0.83	1.00	-0.02
2002m2	0.000	0.04	78	0.00	1.00	86	4	0.90	0.76	1.00	0.08	2011m6	-0.015	0.03	105	-0.42	0.67	121	7	0.94	0.84	0.99	-1.39
2002m3	-0.208	0.05	59	-3.80	0.00	67	4	0.87	0.72	0.81	-18.66	2011m7	0.000	0.03	88	0.00	1.00	102	6	0.94	0.83	1.00	0.06
2002m4	-0.013	0.03	41	-0.39	0.70	48	4	0.95	0.83	0.99	-1.24	2011m9	-0.009	0.03	98	-0.28	0.78	113	6	0.95	0.87	0.99	-0.88
2002m5	-0.092	0.04	45	-2.28	0.03	53	4	0.95	0.85	0.91	-8.68	2011m10	-0.007	0.03	110	-0.23	0.82	125	6	0.95	0.89	0.99	-0.64
2002m6	-0.109	0.05	48	-2.37	0.02	56	4	0.92	0.83	0.90	-10.25	2011m11	-0.009	0.04	82	-0.23	0.82	98	7	0.96	0.92	0.99	-0.84
2002m9	-0.004	0.05	47	-0.08	0.94	55	4	0.92	0.82	1.00	-0.28	2011m12	-0.003	0.03	60	-0.11	0.91	71	3	0.98	0.96	1.00	-0.29
2002m11	-0.416	0.09	34	-4.67	0.00	43	4	0.92	0.90	0.66	-33.64	2012m1	0.000	0.03	58	0.00	1.00	70	3	0.98	0.97	1.00	0.03
2003m1	0.000	0.03	24	0.00	1.00	30	1	0.98	0.98	1.00	0.06	2012m2	-0.013	0.03	58	-0.44	0.66	69	2	0.98	0.97	0.99	-1.26
2003m2	-0.117	0.04	24	-2.75	0.01	30	1	0.97	0.97	0.89	-10.94	2012m3	-0.008	0.03	59	-0.26	0.80	70	2	0.97	0.96	0.99	-0.76
2003m4	-0.111	0.05	22	-2.09	0.05	28	1	0.96	0.96	0.90	-10.33	2012m4	0.000	0.03	68	0.00	1.00	80	3	0.97	0.96	1.00	0.04
2003m7	-0.186	0.05	23	-3.40	0.00	29	1	0.96	0.96	0.83	-16.80	2012m5	0.000	0.03	78	0.00	1.00	90	3	0.97	0.96	1.00	0.03
2003m8	-0.026	0.05	26	-0.53	0.60	32	1	0.96	0.96	0.98	-2.45	2012m6	-0.004	0.02	90	-0.16	0.87	102	3	0.97	0.96	1.00	-0.35
2003m10	-0.082	0.05	28	-1.76	0.09	34	1	0.96	0.96	0.92	-7.80	2012m7	0.000	0.02	102	0.00	1.00	114	3	0.98	0.96	1.00	0.02
2004m2	-0.125	0.06	34	-2.10	0.04	41	2	0.95	0.95	0.88	-11.57	2012m9	-0.001	0.02	118	-0.06	0.95	130	3	0.98	0.96	1.00	-0.11
2004m4	0.009	0.06	37	0.15	0.89	44	2	0.95	0.94	1.01	1.03	2012m10	-0.010	0.02	118	-0.49	0.62	130	3	0.98	0.96	0.99	-1.00
2004m5	0.000	0.06	35	0.00	1.00	42	2	0.95	0.95	1.00	0.18	2012m11	0.005	0.02	102	0.21	0.83	113	3	0.98	0.94	1.01	0.53
2004m6	0.026	0.06	45	0.47	0.64	52	2	0.95	0.95	1.03	2.81	2012m12	0.000	0.02	101	0.00	1.00	112	3	0.98	0.93	1.00	0.03
2004m8	-0.127	0.05	60	-2.77	0.01	67	2	0.95	0.95	0.88	-11.85	2013m1	-0.015	0.02	108	-0.61	0.54	119	3	0.97	0.94	0.99	-1.45
2004m10	0.005	0.04	70	0.14	0.89	77	2	0.95	0.95	1.01	0.59	2013m4	-0.001	0.03	87	-0.03	0.98	98	3	0.97	0.94	1.00	-0.04
2004m12	-0.006	0.04	76	-0.18	0.86	83	2	0.95	0.95	0.99	-0.57	2013m5	0.001	0.04	61	0.02	0.98	70	2	0.96	0.93	1.00	0.15
2005m1	0.000	0.03	77	0.00	1.00	84	2	0.96	0.96	1.00	0.06	2013m6	-0.006	0.03	83	-0.19	0.85	95	4	0.96	0.92	0.99	-0.58
2005m2	-0.016	0.03	75	-0.53	0.60	82	2	0.97	0.97	0.98	-1.58	2013m9	-0.004	0.03	130	-0.15	0.88	145	7	0.96	0.93	1.00	-0.36
2005m3	0.000	0.03	76	0.00	1.00	85	2	0.98	0.98	1.00	0.04	2013m11	-0.002	0.02	150	-0.07	0.95	165	7	0.96	0.93	1.00	-0.13
2005m5	0.002	0.03	75	0.07	0.95	84	2	0.98	0.98	1.00	0.23	2014m1	-0.007	0.02	154	-0.31	0.76	168	7	0.96	0.93	0.99	-0.68
2005m6	-0.034	0.04	80	-0.83	0.41	90	3	0.96	0.95	0.97	-3.26	2014m2	0.000	0.02	160	0.00	1.00	174	7	0.97	0.94	1.00	0.02
2005m7	-0.020	0.04	89	-0.48	0.63	99	3	0.94	0.94	0.98	-1.93	2014m3	0.000	0.02	157	0.00	1.00	171	7	0.97	0.94	1.00	0.02
2005m8	-0.051	0.04	89	-1.32	0.19	98	2	0.94	0.93	0.95	-4.88	2014m4	-0.009	0.02	176	-0.44	0.66	190	7	0.97	0.95	0.99	-0.88
2005m9	0.000	0.04	89	0.00	1.00	98	2	0.95	0.94	1.00	0.07	2014m5	-0.005	0.02	176	-0.26	0.79	189	6	0.97	0.95	1.00	-0.50
2005m12	0.000	0.04	79	0.01	0.99	89	2	0.95	0.94	1.00	0.12	2014m6	0.001	0.02	157	0.04	0.97	170	6	0.97	0.95	1.00	0.09
												2014m7	0.013	0.02	142	0.67	0.51	155	6	0.97	0.94	1.01	1.38

Appendix Table A.5 Other Estimated Regression Coefficients, Intel List Price Hedonic Model without TDP
Color-Coding for Entry and Exit of Characteristics/Microarchitectures from Sample

period ending	lproc	lmaxmhz	lbw	lcores	ht	lcache	int graph	em64t	eist	vt
1996m2	3.06									
1996m5	2.25									
1996m6	2.03									
1996m8	2.28									
1996m11	2.28									
1997m2	2.84									
1997m5	2.83									
1997m8	1.72									
1997m11	1.04									
1998m2	1.10		-0.33							
1998m5	1.60		0.03							
1998m6	2.45		0.24							
1998m7	1.97		0.45							
1998m8	1.63		0.64							
1998m9	2.15		0.55							
1998m10	3.03		0.32							
1998m11	3.32		0.18							
1998m12	3.47		0.11							
1999m1	3.34		0.13							
1999m2	3.54		0.06							
1999m3	3.75									
1999m4	3.46									
1999m5	3.04									
1999m6	2.73									
1999m7	2.47									
1999m8	2.74									
1999m9	3.53		-0.02							
1999m10	3.22		-0.07							
1999m12	2.88		-0.22							
2000m1	3.02		-0.21							
2000m2	3.09		-0.03							
2000m3	2.92		0.01			0.45				
2000m4	2.91		0.00			0.62				
2000m5	2.71		0.07			0.76				
2000m6	2.97		0.01			0.56				
2000m7	3.72		-0.31			0.48				
2000m8	3.21		-0.27			0.66				
2000m10	2.88		-0.26			0.79				
2000m11	2.49		-0.11			0.70				
2000m12	2.26		0.02			0.65				
2001m1	1.83		0.15			0.58				
2001m3	1.47		0.20			0.56				
2001m4	1.35		0.22			0.61				
2001m5	1.17		0.18			0.82				
2001m6	1.09		0.05			1.04				
2001m7	1.39		-0.02			1.06				
2001m8	2.03		-0.29			1.19				
2001m9	2.55		-0.54			1.32				
2001m10	2.35		-0.30			1.30				
2001m12	1.88		-0.10			1.15				
2002m1	1.58		0.03			1.00				
2002m2	1.46		0.13			0.97				
2002m3	1.68		0.57			0.84				
2002m4	2.68		1.95							
2002m5	2.02		1.75			0.60				
2002m6	1.68		1.78			0.53				
2002m9	1.52		1.87			0.45				
2002m11	2.01		1.07		0.39	0.37				
2003m1	2.75		-0.01		0.38	0.35				
2003m2	2.75		0.04		0.43	0.28				
2003m4	2.97		0.06		0.24	0.22				
2003m7	3.24		0.26		0.09	0.30				
2003m8	3.19		0.10		0.17	0.40				
2003m10	2.83		0.11		0.17	0.44				
2004m2	2.54		-0.19		0.17	0.53				
2004m4	2.64		-0.37		0.03	0.62				
2004m5	2.65		-0.31		-0.07	0.65				
2004m6	3.07		-0.31		-0.15	0.64				
2004m8	2.83		-0.31		-0.31	0.73				
2004m10	2.49		-0.30		-0.44	0.81				
2004m12	2.89		-0.18		-0.52	0.79				
2005m1	3.34		-0.07		-0.59	0.78				
2005m2	3.25		-0.09		-0.65	0.84				
2005m3	3.24		-0.13		-0.73	0.92		0.33	-0.68	
2005m5	3.40		-0.21		-0.70	0.91		0.32	-0.69	
2005m6	3.88		-0.63		-0.29	0.79		0.13	-0.46	
2005m7	3.93		-0.45		-0.06	0.60		0.04	-0.23	
2005m8	3.71		1.07		0.40	-0.14		0.06	0.11	
2005m9	3.64		1.80		0.45	-0.37		0.06	0.12	
2005m12	3.72		1.78		0.45	-0.36		0.06	0.11	0.20

period ending	lproc	lmaxmhz	lbw	lcores	ht	lcache	int graph	em64t	eist	vt
2006m1	3.83		1.40		0.36	-0.19		0.04	0.03	0.17
2006m4	3.58		1.49		0.47	-0.15		0.04	0.10	0.05
2006m6	3.34		4.17		0.01	-0.42		0.01	0.30	-0.12
2006m7	3.31		1.45		0.96	-0.36		-0.08	0.39	0.14
2006m10	3.44		1.27		1.06	-0.39		-0.17	0.53	0.29
2006m11	3.76		1.34		0.93	-0.35		-0.21	0.56	0.29
2006m12	4.36		1.88		0.60	-0.37			0.53	
2007m1	4.40		1.64		0.53	-0.38			0.34	-0.87
2007m4	3.32		0.16		0.42	-0.01			-0.21	
2007m5	3.45		0.53		0.43	-0.09				
2007m6	3.37		0.63	1.08	0.30	-0.03				
2007m7	3.26		-2.34	1.06	1.60	-0.08				0.96
2007m9	3.18		-2.22	0.92	1.53	-0.05				0.99
2007m10	2.74		-1.71	0.84	1.30	-0.05				0.97
2007m11	2.19		-1.00	0.87		-0.08				0.85
2008m1	1.95		-0.61	0.53		0.18				0.49
2008m3	1.79		0.14	0.40		0.24				0.23
2008m4	1.86		0.44	0.32		0.27				0.05
2008m7	2.09		1.13	0.33		0.21				-0.34
2008m8	2.09		1.36	0.34		0.20				-0.41
2008m9	2.13		1.17	0.32		0.22				-0.34
2008m10	2.29		1.04	0.28		0.20				-0.26
2008m11	45.56	-43.10	0.78	0.15		0.24				-0.19
2008m12	45.42	-42.95	0.74	0.10		0.32				-0.23
2009m1	47.44	-45.20	1.18	0.11		0.35				-0.26
2009m2	46.86	-44.55	1.45	0.06		0.21				-0.22
2009m3	36.71	-33.26	1.42	-0.15		0.06				-0.29
2009m4	35.59	-32.01	1.37	-0.18		0.10				-0.33
2009m5	33.83	-30.06	1.32	-0.22		0.11				-0.35
2009m6	32.67	-29.19	1.30	-0.25		0.16				-0.34
2009m7	38.24	-35.59	1.23	-0.22		0.25				-0.27
2009m8	46.47	-44.70	1.12	-0.13		0.33				-0.19
2009m9	50.41	-48.76	1.00	-0.10	1.76	0.33				-0.15
2009m10	43.63	-41.83	0.91	-0.15	1.58	0.30				-0.13
2009m11	36.44	-34.38	0.91	-0.27	1.38	0.27				-0.15
2010m1	0.48	2.40	0.74	-0.44	0.21	0.20				-0.21
2010m2	0.38	2.51	0.72	-0.44	0.13	0.22				-0.22
2010m3	0.54	2.54	0.62	-0.49	0.12	0.23				-0.19
2010m4	0.77	2.72	0.26		0.10	0.28				-0.08
2010m5	0.63	2.85	0.20		0.10	0.29				-0.09
2010m6	0.44	2.93	0.16		0.12	0.32				-0.09
2010m7	-0.10	3.43	0.21		0.10	0.32				-0.09
2010m8	-0.81	3.91	0.31		0.08	0.35				-0.11
2010m9	-1.23	3.90	0.36		0.12	0.38				-0.10
2010m10	-1.58	3.94	0.48		0.13	0.40				-0.10
2010m11	-1.72	4.00	0.60		0.13	0.40				-0.13
2011m1	-0.94	3.16	0.66		0.14	0.39	-0.09			-0.14
2011m2	-0.76	2.56	0.74	-0.11	0.18	0.41	-0.08			-0.11
2011m3	-0.79	2.36	0.78	-0.05	0.20	0.42	-0.08			-0.10
2011m4	-0.79	2.36	0.77	-0.06	0.20	0.43	-0.08			-0.12
2011m5	-0.84	2.28	0.73	0.00	0.23	0.44	-0.08			-0.11
2011m6	-0.86	2.23	0.57	0.04	0.24	0.46	-0.06			-0.14
2011m7	-0.75	2.48	0.07	0.34	0.26	0.15	0.06			
2011m9	-0.72	2.21	0.20	0.30	0.29	0.27	0.01		-0.56	
2011m10	-0.69	1.96	0.29	0.31	0.32	0.35	-0.02		-0.57	
2011m11	-0.65	1.63	0.44	0.32	0.34	0.44	-0.05		-0.56	
2011m12	-0.51	1.06	0.91	0.23	0.33	0.63			-0.53	
2012m1	-0.48	1.11	0.97	0.25	0.32	0.60	-0.06		-0.56	
2012m2	-0.52	1.06	1.10	0.46	0.36	0.46	-0.05		-0.56	
2012m3	-0.57	1.13	1.08	0.56	0.38	0.39	-0.06		-0.59	
2012m4	-0.47	1.17	1.11	0.56	0.35	0.36	-0.04		-0.62	
2012m5	-0.40	1.13	1.15	0.58	0.33	0.34	-0.03		-0.63	
2012m6	-0.47	1.24	1.12	0.51	0.34	0.37	-0.04		-0.64	
2012m7	-0.52	1.31	1.09	0.46	0.34	0.40	-0.06		-0.65	
2012m9	-0.44	1.04	1.23	0.50	0.35	0.43	-0.05		-0.63	
2012m10	-0.47	1.01	1.18	0.45	0.36	0.49	-0.04		-0.63	
2012m11	-0.56	1.15	1.06	0.37	0.36	0.53	-0.02			
2012m12	-0.56	1.14	1.05	0.37	0.36	0.54	-0.02			
2013m1	-0.60	1.27	0.81	0.36	0.38	0.57	-0.05			
2013m4	-0.51	1.32	0.61	0.45	0.40	0.52	-0.05			
2013m5	-0.28	1.35		0.74	0.42	0.29	-0.03			
2013m6	-0.34	1.42	0.93	0.68	0.38	0.31	-0.03			
2013m9	-0.39	1.47	0.88	0.55	0.35	0.40	-0.05			
2013m11	-0.42	1.48	0.82	0.49	0.34	0.45	-0.05			
2014m1	-0.47	1.57	0.89	0.42	0.32	0.50				
2014m2	-0.52	1.65	0.92	0.37	0.31	0.52				
2014m3	-0.47	1.57	0.92	0.39	0.32	0.52				
2014m4	-0.43	1.40	0.93	0.43	0.33	0.53				
2014m5	-0.42	1.29	0.94	0.42	0.33	0.56				
2014m6	-0.42	1.24	0.94	0.40	0.33	0.59				
2014m7	-0.35	1.05	1.15	0.57	0.35	0.48				

: microarchitecture enters or exits sample

: non-zero values for indicator vars, lcores; lmaxmhz different from lproc

blank: indicates variable dropped as perfectly collinear

Appendix Table A.6 Regression Summary Statistics, Estimated Time Dummy Coefficients, and Price Relatives
Intel List Price Hedonic Model including TDP

period ending	time dummy	std err	deg of freedom	t-statistic	p value	num obs	number arch fixed effects	r2 total	r2 within	bias-corrected price relative	pct change from prev observation	period ending	time dummy	std err	deg of freedom	t-statistic	p value	num obs	number arch fixed effects	r2 total	r2 within	bias-corrected price relative	pct change from prev observation
1998m10	-0.13	0.06	1	-2.37	0.25	4	1	0.95	0.95	0.88	-12.27	2007m4	-0.09	0.05	44	-1.85	0.07	57	6	0.98	0.88	0.92	-8.28
1998m11	0.00	0.00	1	0.02	0.99	4	1	1.00	1.00	1.00	0.00	2007m5	-0.07	0.05	44	-1.32	0.20	56	6	0.97	0.84	0.94	-6.42
1998m12	-0.41	0.02	1	-26.25	0.02	4	1	1.00	1.00	0.66	-33.74	2007m6	-0.02	0.06	45	-0.32	0.75	57	5	0.97	0.89	0.98	-1.64
1999m1	-0.21	0.02	2	-8.53	0.01	6	1	1.00	1.00	0.81	-18.62	2007m7	-0.05	0.06	54	-0.92	0.36	67	5	0.95	0.88	0.95	-5.06
1999m2	-0.23	0.03	5	-7.56	0.00	10	2	1.00	0.99	0.79	-20.84	2007m9	-0.02	0.06	62	-0.39	0.70	75	5	0.95	0.87	0.98	-2.01
1999m3	-0.01	0.02	7	-0.34	0.74	12	2	1.00	0.99	0.99	-0.57	2007m10	-0.07	0.06	49	-1.07	0.29	61	4	0.95	0.89	0.94	-6.33
1999m4	-0.17	0.04	7	-4.12	0.00	12	2	1.00	0.97	0.85	-15.16	2007m11	0.00	0.03	38	0.00	1.00	48	3	0.98	0.97	1.00	0.06
1999m5	-0.12	0.08	8	-1.41	0.20	13	2	0.98	0.88	0.89	-10.61	2008m1	0.00	0.04	47	-0.08	0.94	59	5	0.97	0.94	1.00	-0.26
1999m6	-0.04	0.08	9	-0.51	0.62	14	2	0.98	0.86	0.96	-3.87	2008m3	-0.02	0.04	60	-0.40	0.69	72	5	0.97	0.93	0.99	-1.49
1999m7	-0.06	0.09	9	-0.63	0.55	14	2	0.97	0.82	0.95	-5.21	2008m4	-0.08	0.04	60	-1.86	0.07	71	4	0.97	0.93	0.93	-7.24
1999m8	-0.21	0.09	9	-2.42	0.04	14	2	0.98	0.91	0.81	-18.74	2008m7	-0.06	0.04	55	-1.44	0.16	66	4	0.98	0.94	0.95	-5.32
1999m9	-0.18	0.04	9	-4.40	0.00	15	2	0.99	0.98	0.84	-16.43	2008m8	-0.01	0.03	60	-0.28	0.78	71	4	0.98	0.95	0.99	-0.84
1999m10	-0.12	0.04	16	-2.64	0.02	23	3	0.99	0.96	0.89	-10.82	2008m9	0.00	0.03	67	-0.05	0.96	78	4	0.98	0.95	1.00	-0.10
1999m12	-0.04	0.03	25	-1.37	0.18	32	3	0.99	0.96	0.96	-3.58	2008m10	-0.05	0.03	61	-1.55	0.13	72	4	0.98	0.96	0.95	-4.60
2000m1	-0.06	0.03	28	-2.14	0.04	35	3	0.99	0.96	0.94	-6.13	2008m11	0.00	0.03	59	-0.13	0.90	72	5	0.99	0.97	1.00	-0.30
2000m2	-0.36	0.04	25	-9.82	0.00	32	3	0.98	0.95	0.70	-30.01	2008m12	-0.01	0.03	57	-0.30	0.77	70	5	0.99	0.97	0.99	-0.75
2000m3	0.00	0.03	35	0.10	0.92	43	3	0.99	0.98	1.00	0.31	2009m1	-0.05	0.06	52	-0.92	0.36	65	5	0.96	0.84	0.95	-4.82
2000m4	-0.18	0.03	50	-5.44	0.00	58	3	0.97	0.95	0.84	-16.09	2009m2	-0.02	0.06	52	-0.30	0.77	65	5	0.95	0.79	0.98	-1.51
2000m5	-0.17	0.05	52	-3.66	0.00	60	3	0.94	0.90	0.84	-15.82	2009m3	0.00	0.06	48	0.00	1.00	60	4	0.95	0.81	1.00	0.16
2000m6	-0.07	0.05	52	-1.46	0.15	60	3	0.94	0.90	0.93	-6.84	2009m4	-0.03	0.05	49	-0.61	0.55	61	4	0.96	0.83	0.97	-3.14
2000m7	-0.08	0.03	50	-2.72	0.01	58	3	0.98	0.97	0.93	-7.42	2009m5	0.00	0.05	51	-0.04	0.97	63	4	0.96	0.84	1.00	-0.06
2000m8	-0.16	0.04	51	-4.37	0.00	59	3	0.96	0.94	0.85	-14.61	2009m6	-0.01	0.05	56	-0.26	0.80	68	4	0.96	0.84	0.99	-1.12
2000m10	-0.12	0.03	51	-3.81	0.00	59	3	0.97	0.96	0.89	-10.85	2009m7	-0.08	0.04	57	-1.82	0.07	69	4	0.97	0.85	0.93	-7.28
2000m11	-0.14	0.03	50	-4.80	0.00	58	3	0.97	0.96	0.87	-12.61	2009m8	0.00	0.02	55	-0.16	0.87	67	4	0.99	0.95	1.00	-0.30
2000m12	-0.03	0.03	52	-0.94	0.35	60	3	0.97	0.95	0.97	-2.57	2009m9	0.01	0.02	59	0.29	0.77	73	5	0.99	0.95	1.01	0.65
2001m1	-0.13	0.03	55	-4.50	0.00	63	3	0.96	0.93	0.87	-12.58	2009m10	-0.02	0.02	63	-0.69	0.49	77	5	0.99	0.94	0.98	-1.64
2001m3	-0.07	0.02	53	-2.87	0.01	60	2	0.97	0.95	0.94	-6.49	2009m11	0.00	0.03	62	0.00	1.00	76	5	0.98	0.93	1.00	0.03
2001m4	-0.13	0.03	47	-4.29	0.00	54	2	0.95	0.92	0.88	-12.43	2010m1	-0.01	0.03	73	-0.43	0.67	88	6	0.97	0.87	0.99	-1.39
2001m5	-0.11	0.03	43	-3.84	0.00	50	2	0.96	0.93	0.90	-10.43	2010m2	-0.01	0.03	86	-0.38	0.71	101	6	0.97	0.86	0.99	-1.10
2001m6	0.00	0.02	40	-0.09	0.93	47	2	0.97	0.96	1.00	-0.17	2010m3	-0.02	0.03	79	-0.45	0.66	94	6	0.96	0.86	0.99	-1.45
2001m7	0.02	0.03	43	0.48	0.63	50	2	0.95	0.92	1.02	1.66	2010m4	0.00	0.03	72	0.01	0.99	87	7	0.97	0.88	1.00	0.08
2001m8	-0.16	0.04	52	-4.05	0.00	60	3	0.96	0.92	0.86	-14.49	2010m5	-0.01	0.03	77	-0.24	0.81	91	6	0.96	0.87	0.99	-0.76
2001m9	-0.11	0.03	63	-3.15	0.00	71	3	0.95	0.91	0.90	-10.27	2010m6	0.00	0.03	82	0.00	1.00	96	6	0.96	0.86	1.00	0.06
2001m10	-0.06	0.04	69	-1.64	0.10	77	3	0.92	0.88	0.94	-6.08	2010m7	-0.04	0.03	82	-1.04	0.30	96	6	0.96	0.85	0.97	-3.48
2001m12	-0.08	0.04	70	-2.19	0.03	78	3	0.91	0.86	0.92	-7.80	2010m8	-0.01	0.03	86	-0.38	0.70	100	6	0.95	0.84	0.99	-1.24
2002m1	-0.02	0.03	73	-0.55	0.58	82	4	0.93	0.85	0.98	-1.78	2010m9	-0.01	0.03	87	-0.19	0.85	101	6	0.96	0.83	0.99	-0.59
2002m2	0.00	0.03	77	0.00	1.00	86	4	0.94	0.85	1.00	0.05	2010m10	-0.01	0.03	84	-0.43	0.67	98	6	0.96	0.84	0.99	-1.35
2002m3	-0.20	0.04	58	-4.66	0.00	67	4	0.92	0.83	0.82	-18.38	2010m11	0.00	0.03	85	-0.08	0.94	99	6	0.96	0.84	1.00	-0.22
2002m4	-0.01	0.03	40	-0.38	0.70	48	4	0.95	0.83	0.99	-1.24	2011m1	0.00	0.03	95	0.00	1.00	111	7	0.95	0.83	1.00	0.05
2002m5	-0.08	0.03	44	-2.40	0.02	53	4	0.96	0.89	0.92	-7.95	2011m2	-0.01	0.03	108	-0.37	0.71	125	7	0.95	0.82	0.99	-1.08
2002m6	-0.10	0.04	47	-2.77	0.01	56	4	0.95	0.89	0.90	-9.86	2011m3	0.00	0.03	110	0.01	0.99	127	7	0.94	0.82	1.00	0.08
2002m9	0.01	0.04	46	0.17	0.87	55	4	0.95	0.89	1.01	0.69	2011m4	0.00	0.03	109	0.00	1.00	126	7	0.94	0.82	1.00	0.05
2002m11	-0.43	0.09	33	-4.78	0.00	43	4	0.93	0.90	0.66	-34.25	2011m5	0.00	0.03	116	0.09	0.93	133	7	0.94	0.84	1.00	0.30
2003m1	0.00	0.03	23	0.00	1.00	30	1	0.99	0.99	1.00	0.05	2011m6	-0.02	0.03	104	-0.54	0.59	121	7	0.94	0.85	0.98	-1.73
2003m2	-0.12	0.04	23	-2.97	0.01	30	1	0.98	0.98	0.89	-10.95	2011m7	0.00	0.03	87	0.00	1.00	102	6	0.95	0.85	1.00	0.05
2003m4	-0.10	0.05	21	-2.24	0.04	28	1	0.97	0.97	0.90	-9.84	2011m9	-0.01	0.03	97	-0.40	0.69	113	6	0.96	0.89	0.99	-1.17
2003m7	-0.17	0.05	22	-3.12	0.01	29	1	0.97	0.97	0.85	-15.43	2011m10	-0.01	0.03	109	-0.26	0.80	125	6	0.96	0.91	0.99	-0.66
2003m8	-0.03	0.04	25	-0.58	0.56	32	1	0.97	0.97	0.98	-2.47	2011m11	-0.01	0.03	81	-0.29	0.78	98	7	0.97	0.94	0.99	-0.92
2003m10	-0.09	0.04	27	-1.98	0.06	34	1	0.97	0.97	0.92	-8.11	2011m12	0.00	0.03	59	0.18	0.85	71	3	0.99	0.97	1.00	0.49
2004m2	-0.16	0.05	33	-3.00	0.01	41	2	0.96	0.96	0.86	-14.39	2012m1	0.00	0.02	57	0.07	0.94	70	3	0.99	0.98	1.00	0.20
2004m4	0.00	0.05	36	0.02	0.99	44	2	0.97	0.96	1.00	0.19	2012m2	-0.01	0.03	57	-0.49	0.62	69	2	0.98	0.97	0.99	-1.27
2004m5	0.00	0.05	34	0.00	1.00	42	2	0.97	0.96	1.00	0.12	2012m3	-0.01	0.03	58	-0.27	0.79	70	2	0.98	0.97	0.99	-0.76
2004m6	0.03	0.05	44	0.60	0.55	52	2	0.96	0.96	1.03	3.09	2012m4	0.00	0.03	67	0.00	1.00	80	3	0.98	0.97	1.00	0.04
2004m8	-0.11	0.04	59	-2.73	0.01	67	2	0.96	0.96	0.89	-10.63	2012m5	0.00	0.02	77	0.00	1.00	90	3	0.98	0.96	1.00	0.03
2004m10	0.00	0.04	69	-0.04	0.97	77	2	0.96	0.96	1.00	-0.07	2012m6	-0.01	0.02	89	-0.42	0.67	102	3	0.98	0.97	0.99	-0.94
2004m12	0.00	0.03	75	-0.14	0.89	83	2	0.96	0.96	1.00	-0.42	2012m7	0.00	0.02	101	0.00	1.00	114	3	0.98	0.97	1.00	0.02
2005m1	0.00	0.03	76	0.00	1.00	84	2	0.97	0.97	1.00	0.05	2012m9	0.00	0.02	117	-0.13	0.90	130	3	0.98	0.97	1.00	-0.24
2005m2	-0.02	0.03	74	-0.61	0.54	82	2	0.97	0.97	0.98	-1.73	2012m10	-0.01	0.02	117	-0.65	0.52	130	3	0.98	0.97	0.99	-1.26
2005m3	0.00	0.03	75	0.00	1.00	85	2	0.98	0.98	1.00	0.03	2012m11	0.00	0.02	101	0.21	0.83	113	3	0.98	0.95	1.00	0.49
2005m5	0.00	0.03	74	0.08	0.93	84	2	0.98	0.98	1.00	0.24	2012m12	0.00	0.02	100	0.00	1.00	112	3	0.98	0.94	1.00	0.03
2005m6	-0.03	0.04	79	-0.96	0.34	90	3	0.97	0.96	0.97	-3.32	2013m1	-0.01	0.02	107	-0.54	0.59	119	3	0.98	0.95	0.99	-1.20
2005m7	-0.03	0.04	88	-0.70	0.49	99	3	0.96	0.96	0.98	-2.45	2013m4	0.00	0.03	86	-0.06	0.96	98	3	0.97	0.95	1.00	-0.13
2005m8	-0.05	0.03	88	-1.49	0.14	98	2	0.95	0.95	0.95	-4.90	2013m5	0.00	0.03	60	0.02	0.98	70	2	0.97	0.94	1.00	0.14
2005m9	0.00	0.03	88	0.00	1.00	98	2	0.96	0.95	1.00	0.05	2013m6	-0.01	0.03	82	-0.43	0.67	95	4	0.97	0.94	0.99	-1.25
2005m12	0.01	0.04	78	0.42	0.68	89	2	0.96	0.95	1.02	1.56	2013m9	-0.01	0.02	129	-0.42	0.68	145	7	0.97	0.94	0.99	-0.93
2006m1	0.00	0.04	77	-0.11	0.92	90	4	0.96	0.95	1.00	-0.32	2013m11	0.00	0.02	149	-0.14	0.89	165	7	0.97	0.94	1.00	-0.28
2006m4	-0.22	0.04	76	-5.48	0.00	89	4	0.95	0.94	0.80	-19.81	2014m1	-0.01	0.02	153	-0.32	0.75	168	7	0.97	0.94	0.99	-0.66
2006m6	0.01	0.03	67	0.32	0.75	80	4	0.98	0.97	1.01	1.10	2014m2	0.00	0.02	159	0.00	1.00	174	7	0.97	0.95	1.00	0.02
2006m7	-0.18	0.05	77	-3.60	0.00	91	5	0.95	0.93	0.84	-15.96	2014m3	0.00	0.02	156	0.00	1.00	171	7	0.97	0.95	1.00	0.02
2006m10	-0.04	0.05	87	-0.82	0.41	101	5	0.93	0.90	0.96	-4.04	2014m4	-0.02	0.02	175	-0.79	0.43	190	7	0.97	0.95	0.99	-1.49
2006m11	-0.02	0.06	68	-0.35	0.73	82	5	0.93	0.91	0.98	-2.00	2014m5	0.00	0.02	175	-0.06	0.96	189	6	0.97	0.96	1.00	-0.09
2006m12	0.00	0.06	51	0.00	1.00	64	6	0.95	0.92	1.00	0.17	2014m6	0.00	0.02	156	0.04	0.97	170	6	0.97	0.95	1.00	0.09
2007m1	-0.30	0.08	47	-3.86	0.00	61	6	0.93	0.86	0.74	-25.54	2014m7	0.01	0.02	141	0.56	0.57	155	6	0.97	0.95	1.01	1.09

Appendix Table A.7 Other Estimated Regression Coefficients, Intel List Price Hedonic Model including TDP
Color-Coding for Entry and Exit of Characteristics/Microarchitectures from Sample

period ending	lproc	lmaxmhz	lbw	lcores	ht	lcache	int graph	ltdp	em64t	eist	vt
1998m10	1.89										
1998m11	1.36										
1998m12	1.51										
1999m1	-28.12							30.98			
1999m2	3.83							-0.86			
1999m3	3.38							-0.14			
1999m4	4.12							-1.14			
1999m5	4.15							-0.91			
1999m6	2.06							1.60			
1999m7	0.71							2.85			
1999m8	1.62							2.21			
1999m9	2.96		0.10					1.25			
1999m10	3.80		-0.10					-0.25			
1999m12	3.14		-0.24					-0.06			
2000m1	3.09		-0.23					0.10			
2000m2	3.30		-0.04					-0.15			
2000m3	3.19		0.04			0.39		-0.28			
2000m4	3.34		0.06			0.52		-0.40			
2000m5	3.10		0.11			0.67		-0.34			
2000m6	3.00		0.01			0.56		-0.02			
2000m7	3.22		-0.45			0.58		0.54			
2000m8	2.81		-0.38			0.74		0.45			
2000m10	2.69		-0.31			0.83		0.21			
2000m11	2.26		-0.17			0.75		0.25			
2000m12	1.89		-0.07			0.73		0.39			
2001m1	1.66		0.12			0.60		0.17			
2001m3	1.48		0.20			0.56		0.00			
2001m4	1.34		0.21			0.61		0.00			
2001m5	1.30		0.21			0.80		-0.14			
2001m6	1.31		0.10			1.02		-0.22			
2001m7	1.66		0.04			1.02		-0.27			
2001m8	2.68		-0.15			1.12		-0.70			
2001m9	4.60		-0.11			1.20		-2.22			
2001m10	5.33		0.24			1.15		-3.21			
2001m12	4.96		0.40			1.02		-3.29			
2002m1	4.45		0.47			0.88		-3.06			
2002m2	4.35		0.56			0.85		-3.07			
2002m3	4.90		0.74			0.85		-3.52			
2002m4	2.69		1.95					-0.01			
2002m5	7.06		0.93			-0.85		-7.24			
2002m6	8.41		0.79			-1.41		-9.75			
2002m9	8.46		0.94			-1.53		-9.89			
2002m11	2.30		1.09		0.52	0.32		-0.66			
2003m1	2.75		-0.11		0.20	0.34		0.68			
2003m2	2.75		-0.06		0.24	0.27		0.70			
2003m4	2.84		-0.05		-0.01	0.21		1.09			
2003m7	1.88		0.26		-0.09	0.31		1.70			
2003m8	1.22		0.34		-0.15	0.35		2.61			
2003m10	1.05		0.31		-0.11	0.40		2.32			
2004m2	0.32		0.26		-0.19	0.38		2.73			
2004m4	-0.08		0.19		-0.32	0.37		3.32			
2004m5	0.03		0.18		-0.36	0.39		3.24			
2004m6	1.40		-0.03		-0.29	0.48		1.97			
2004m8	1.65		-0.16		-0.36	0.62		1.35			
2004m10	1.68		-0.25		-0.43	0.73		0.93			
2004m12	2.22		-0.21		-0.49	0.73		0.80			
2005m1	2.70		-0.12		-0.55	0.71		0.76			
2005m2	2.73		-0.13		-0.60	0.78		0.63			
2005m3	2.81		-0.16		-0.67	0.86		0.50	0.34	-0.63	
2005m5	2.87		-0.27		-0.62	0.85		0.60	0.35	-0.63	
2005m6	2.86		-0.96		-0.23	0.78		1.07	0.19	-0.46	
2005m7	2.97		-1.00		-0.04	0.70		1.07	0.06	-0.28	
2005m8	2.97		0.03		0.24	0.24		0.95	0.05	-0.11	
2005m9	2.91		0.77		0.29	0.01		0.93	0.04	-0.10	
2005m12	2.96		0.68		0.27	0.04		0.99	0.03	-0.12	0.07
2006m1	3.02		0.47		0.23	0.12		1.04	0.00	-0.16	0.05
2006m4	2.88		0.86		0.41	0.02		0.86	0.02	-0.03	-0.02
2006m6	2.66		1.81		0.44	-0.08		0.90	-0.05	0.09	-0.20
2006m7	2.55		1.28		0.67	-0.12		1.32	-0.23	0.18	-0.05
2006m10	2.74		1.08		0.78	-0.17		1.32	-0.32	0.33	0.08
2006m11	2.92		1.13		0.59	-0.07		1.52	-0.40	0.33	0.05
2006m12	3.38		1.55		0.28	-0.07		1.65		0.35	
2007m1	3.87		1.30		0.42	-0.27		1.50		0.30	-0.69
2007m4	3.32		0.16		0.41	-0.03		0.54		-0.16	
2007m5	3.39		0.54		0.36	-0.11		0.71			
2007m6	3.30		0.64	0.34	0.21	-0.04		0.85			
2007m7	3.17		-2.32	-0.07	1.45	-0.08		1.27			0.96
2007m9	3.06		-2.23	-0.54	1.33	-0.04		1.63			0.99
2007m10	2.57		-1.83	-1.07	1.05	-0.01		2.09			1.00
2007m11	1.79		-1.44	-2.86		0.07		3.99			0.94
2008m1	1.50		-0.78	-2.29		0.25		3.12			0.55
2008m3	1.26		-0.51	-2.32		0.34		3.03			0.42
2008m4	1.15		-0.55	-2.36		0.42		2.98			0.35
2008m7	1.17		-0.11	-2.28		0.43		2.90			0.07
2008m8	1.24		0.51	-2.21		0.35		2.90			-0.14
2008m9	1.32		0.55	-2.25		0.33		2.94			-0.14
2008m10	1.37		0.46	-2.23		0.32		2.86			-0.08
2008m11	55.10	-53.71	0.33	-2.20		0.34		2.73			-0.01
2008m12	55.09	-53.70	0.36	-2.20		0.33		2.71			-0.01
2009m1	52.49	-50.81	1.01	-0.95		0.34		1.23			-0.19
2009m2	49.51	-47.50	1.38	-0.43		0.24		0.55			-0.22
2009m3	40.11	-37.05	1.37	-0.52		0.10		0.45			-0.28
2009m4	38.80	-35.58	1.33	-0.56		0.11		0.47			-0.30
2009m5	36.88	-33.46	1.29	-0.59		0.12		0.47			-0.33
2009m6	35.74	-32.58	1.27	-0.64		0.16		0.49			-0.31
2009m7	38.81	-36.21	1.22	-0.36		0.25		0.17			-0.26
2009m8	47.09	-45.37	1.07	0.39		0.34		-0.58			-0.17
2009m9	51.11	-49.53	0.96	0.44	1.78	0.34		-0.60			-0.13
2009m10	44.47	-42.75	0.88	0.40	1.61	0.32		-0.60			-0.12
2009m11	37.42	-35.46	0.87	0.28	1.42	0.29		-0.60			-0.13
2010m1	0.92	1.99	0.70	0.11	0.23	0.21		-0.62			-0.20
2010m2	0.83	2.15	0.67	0.12	0.15	0.22		-0.65			-0.21
2010m3	1.00	2.18	0.59	0.07	0.14	0.22		-0.66			-0.19
2010m4	1.26	2.35	0.25		0.11	0.26		-0.66			-0.08
2010m5	1.10	2.50	0.18		0.12	0.28		-0.65			-0.09
2010m6	0.88	2.60	0.14		0.13	0.31		-0.63			-0.10
2010m7	0.41	3.05	0.20		0.11	0.32		-0.64			-0.10
2010m8	-0.31	3.54	0.29		0.09	0.34		-0.62			-0.12
2010m9	-0.78	3.57	0.35		0.12	0.37		-0.56			-0.10
2010m10	-1.16	3.64	0.46		0.13	0.39		-0.52			-0.10
2010m11	-1.31	3.71	0.59		0.13	0.39		-0.50			-0.14
2011m1	-0.35	2.70	0.65		0.15	0.38	-0.07	-0.34			-0.14
2011m2	0.03	2.02	0.72	0.28	0.18	0.39	-0.06	-0.39			-0.13
2011m3	0.11	1.82	0.76	0.37	0.19	0.40	-0.06	-0.44			-0.12
2011m4	0.10	1.82	0.75	0.37	0.19	0.40	-0.06	-0.44			-0.13
2011m5	0.17	1.71	0.71	0.42	0.20	0.41	-0.05	-0.47			-0.13
2011m6	0.23	1.68	0.55	0.45	0.20	0.41	-0.03	-0.49			-0.17
2011m7	0.80	1.83	-0.05	0.99	0.20	-0.01	0.13	-0.67			
2011m9	0.95	1.66	-0.02	1.01	0.20	0.05	0.12	-0.72		-1.05	
2011m10	1.10	1.49	0.00	1.07	0.21	0.08	0.11	-0.76		-1.12	
2011m11	1.20	1.21	0.06	1.06	0.22	0.17	0.10	-0.76		-1.13	
2011m12	0.54	0.83	0.59	0.56	0.27	0.55		-0.48		-0.82	
2012m1	0.36	0.84	0.70	0.48	0.28	0.59	-0.05	-0.41		-0.75	
2012m2	0.28	0.77	0.81	0.66	0.32	0.47	-0.05	-0.39		-0.73	
2012m3	0.09	0.89	0.85	0.72	0.35	0.40	-0.05	-0.32		-0.73	
2012m4	0.06	0.98	0.92	0.70	0.32	0.37	-0.04	-0.27		-0.74	
2012m5	0.15	0.93	0.95	0.73	0.31	0.35	-0.03	-0.29		-0.75	
2012m6	0.04	1.09	0.92	0.69	0.32	0.35	-0.05	-0.27		-0.78	
2012m7	0.00	1.19	0.87	0.66	0.33	0.36	-0.06	-0.27		-0.80	
2012m9	-0.02	0.95	1.06	0.65	0.35	0.41	-0.05	-0.23		-0.76	
2012m10	-0.10	0.96	1.00	0.59	0.35	0.47	-0.05	-0.22		-0.76	
2012m11	-0.16	1.14	0.82	0.51	0.35	0.51	-0.02	-0.25			
2012m12	-0.16	1.14	0.81	0.50	0.35	0.52	-0.02	-0.25			
2013m1	-0.14	1.26	0.57	0.51	0.36	0.54	-0.05	-0.28			
2013m4	0.09	1.27	0.34	0.65	0.37	0.47	-0.04	-0.36			
2013m5	1.16	1.08		1.24	0.32	0.20	0.04	-0.78			
2013m6	1.01	1.05	0.45	1.28	0.32	0.16	0.04	-0.72			
2013m9	0.66	1.27	0.74	1.08	0.30	0.24	0.02	-0.58			
2013m11	0.54	1.38	0.71	0.98	0.29	0.31	0.01	-0.55			
2014m1	0.36	1.52	0.78	0.84	0.27	0.37		-0.49			
2014m2	0.20	1.62	0.83	0.73	0.26	0.41		-0.43			
2014m3	0.35	1.52	0.80	0.81	0.26	0.39		-0.49			
2014m4	0.44	1.30	0.78	0.87	0.27	0.41		-0.49			
2014m5	0.34	1.23	0.79	0.81	0.28	0.45		-0.43			
2014m6	0.28	1.25	0.78	0.77	0.28	0.48		-0.41			
2014m7	0.41	0.98	0.90	0.93	0.29	0.42		-0.43			

: microarchitecture enters or exits sample

: non-zero values for indicator vars, lcores; lmaxmhz different from lproc

blank: indicates variable dropped as perfectly collinear